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Catalog
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Intel FPGA and Custom Logic Solutions Portfolio

Intel delivers a broad portfolio of custom logic solutions — FPGAs, SoCs, structured ASICs, and CPLDs—together with software tools, intellectual property (IP), embedded processors, customer support, and technical training. Intel's product leadership, excellent value, and superior quality of service give you a measurable advantage. Bring your great ideas to life faster, better, and more cost effectively.

FPGAs, Structured ASICs, and CPLDs

Intel FPGAs and CPLDs give you the flexibility to innovate, differentiate, and stay ahead in the market. We have five classes of FPGAs to meet your market needs, from the industry's highest density and performance to the most cost effective.

Intel Agilex FPGAs

The Intel Agilex portfolio presents a broad range of product offerings that address the full breadth of programmable logic needs across every technology sector from edge and embedded, to communications and data centers.

Intel Cyclone Series

The Intel Cyclone FPGA series is built to meet your low-power, cost-sensitive design needs, enabling you to get to market faster.

Intel Stratix Series

The Intel Stratix FPGA and SoC family enables you to deliver high-performance, state-of-the-art products to market faster with lower risk and higher productivity.

Intel MAX Series

The Intel MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single-chip small form.

Intel Arria Series

The Intel Arria device family delivers performance and power efficiency in the midrange.

Intel eASIC Devices

Intel eASIC structured ASIC devices complete the gap between FPGA and ASIC by delivering lower power and lower unit price versus FPGAs and lower non-recurring engineering (NRE) and faster time to market versus standard cell ASICs.

Acceleration Platform or Card Solutions

Intel FPGA-based acceleration platforms or cards enable a scalable volume deployment of various workloads in edge, network, cloud, enterprise, and other types of data center environment through Intel FPGA Programmable Acceleration Cards (Intel FPGA PACs) and development software, such as the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs and the OpenVINO™ toolkit.

Productivity-Enhancing Design Software, Embedded Processing, IP, Development Kits, and Training

With Intel, you get a complete design environment and a wide choice of design tools—all built to work together so your designs are up and running fast. You can try one of our training classes to get a jump-start on your designs. Choose Intel and see how we enhance your productivity and make a difference to your bottom line.

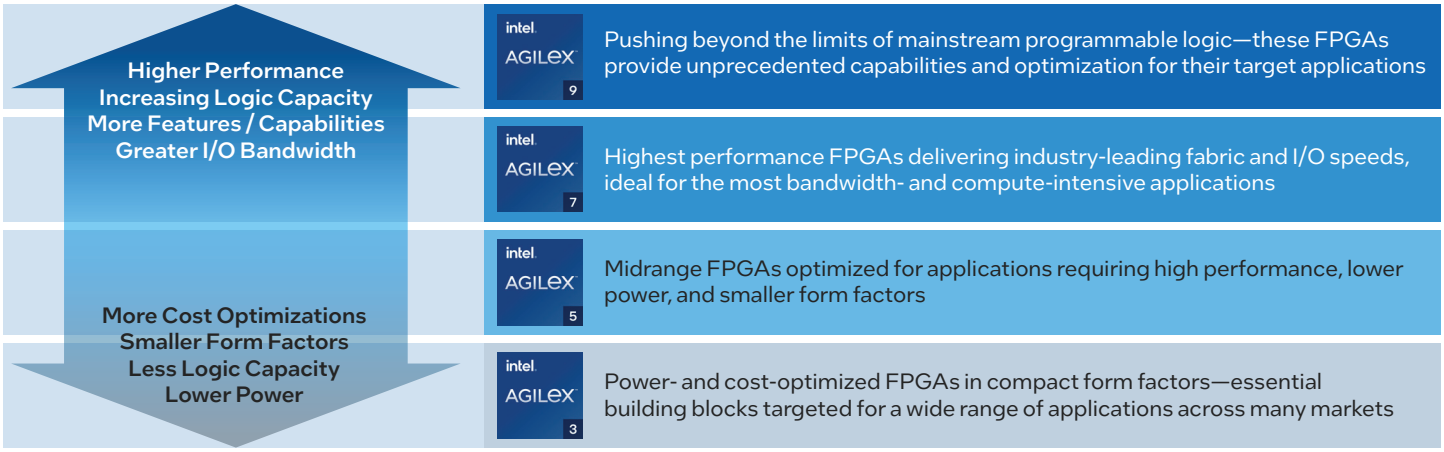
Intel Agilex FPGAs and SoCs:

A Comprehensive Programmable Logic Portfolio for the Connected World

intel.com/agilex

The Intel Agilex FPGA portfolio presents a broad range of product offerings that address the full breadth of programmable logic needs across every technology sector from edge and embedded, to communications and data centers. In all these sectors, a data explosion is driving demand for new products to move, process, and store data, as well as derive actionable insights from it. The developers of these products need hardware flexibility to address the challenges of changing market requirements, integrating multiple functions, adopting evolving standards, and supporting diverse workloads. Intel Agilex FPGAs provide the flexibility needed to tackle these challenges, as well as advanced application-optimized features and capabilities that help developers deliver innovation with agility.

The Intel Agilex FPGA Portfolio



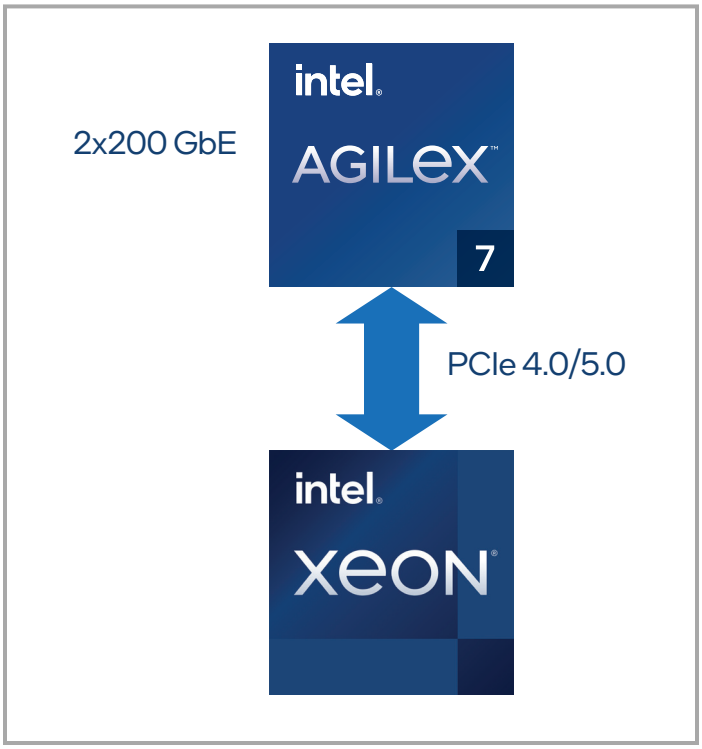
Intel Agilex 7 FPGA and SoC Overview

Intel Agilex 7 Devices

The Intel Agilex 7 devices include the industry's highest performance FPGAs providing a range of premium features for the most demanding applications, including the F-Series, I-Series, and M-Series. This tier offers the industry's highest data rate transceivers—up to 116 Gbps—the first PCI Express* (PCIe*) 5.0 and Compute Express Link (CXL) support, and options to integrate in-package HBM2E memory delivering the industry's highest memory bandwidth (over 1 TBps). These capabilities enable customized connectivity and acceleration for the most compute, bandwidth, and memory-intensive use cases in communications, data center, defense, high-performance computing, video, high-end test/measurement/medical, and more.

F-Series FPGAs and SoCs	I-Series FPGAs and SoCs	M-Series FPGAs and SoCs
F-Series devices are general purpose FPGAs built on the Intel 10 nm SuperFin process technology. With features including transceiver rates up to 58 Gbps, advanced digital signal processing (DSP) blocks supporting multiple precisions of fixed-point and floating-point operations, and high-performance crypto blocks, they are ideal for a wide range of applications across many markets.	I-Series devices offer the highest-performance I/O interfaces to address bandwidth-intensive applications. Manufactured on the Intel 10 nm SuperFin process technology, this series builds upon the F-Series device features offering transceiver rates up to 116 Gbps, PCIe 5.0 support, and cache- and memory-coherent attach to processors with CXL.	M-Series devices are optimized for compute- and memory-intensive applications. Leveraging the Intel 7 process technology, this series builds upon I-Series device features offering an extensive memory hierarchy including integrated high-bandwidth memory (HBM) and high-efficiency interfaces to DDR5 memory with a hard memory Network-on-Chip (NoC) to maximize memory bandwidth.

Efficient Network Transformation



Datapath Acceleration

VNF Performance Optimization

- Load balancing
- Data integrity
- Network translation

Significant Improvements

- Throughput
- Jitter
- Latency

Infrastructure Offload

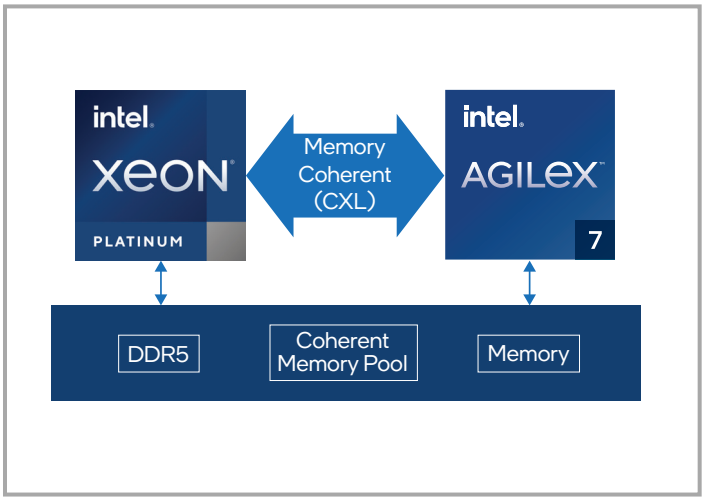
Optimized Architecture

- Infrastructure Processing Unit (IPU)
- vRouter
- Security

Small Form Factor and Low Power

- Wide range of servers

Converged Workload Acceleration for the Data Center

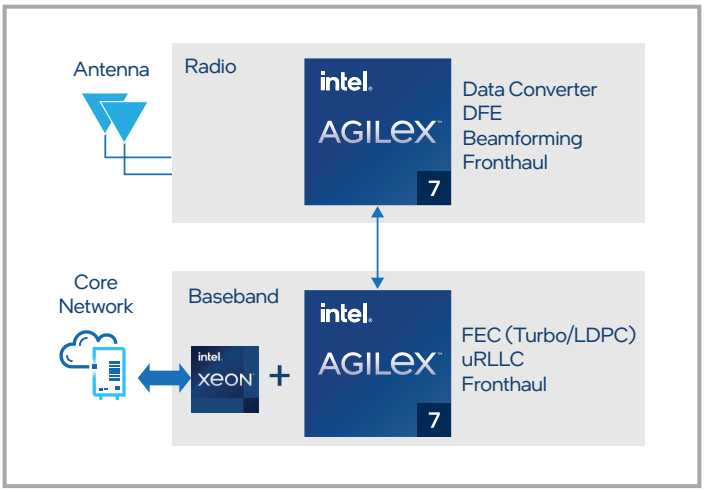


Infrastructure Acceleration
- Network
- Security
- Remote memory access

Application Acceleration
- Artificial intelligence (AI)
- Search
- Video transcode
- Database
- 38 TFLOPs of DSP performance[1]

Storage Acceleration
- Compression
- Decompression
- Encryption
- Memory hierarchy management

Agility and Flexibility for All Stages of 5G Implementation



Custom Logic Continuum

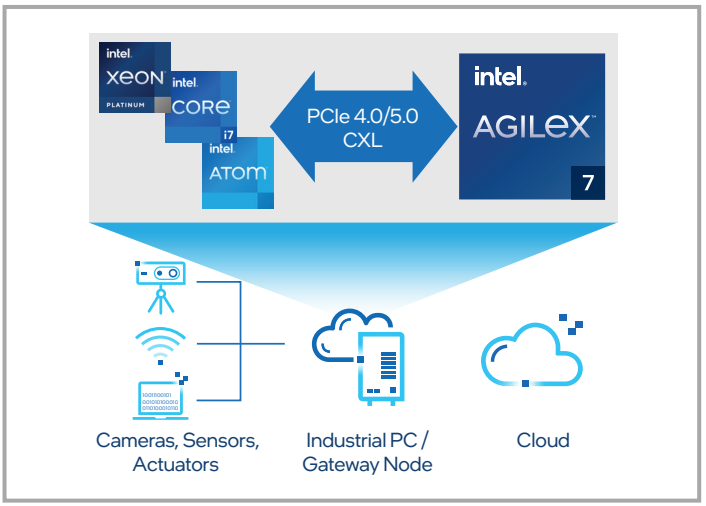
FPGA Flexibility
- High flexibility
- Short time to market

Rapid Intel eASIC Device Optimization
- Power and cost optimization

Full Custom ASIC Optimization
- Best power[1]
- Best performance[1]
- Best cost[1]

Application-Specific Tile Options
- Data converter
- Vector engine
- Custom compute

Smart, Safe, and Secure Factory Acceleration



Acceleration and Analytics
- In-line protocol acceleration
- Look-aside application acceleration

Safety and Security
- Secure boot
- Encryption
- Authentication

Customized Connectivity
- Time-sensitive networks
- Flexible I/O

Product and Performance Information:
[1] This comparison is based on the Intel Agilex FPGA and SoC family vs. Intel Stratix 10 FPGA using simulation results and is subject to change. This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications, and roadmaps.

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Devices: Intel Agilex FPGA Portfolio

Intel Agilex 7 FPGA and SoC F-Series Features

View device ordering codes on page 55.

Product Line		AGF 006	AGF 008	AGF 012	AGF 014	AGF 019	AGF 023	AGF 022	AGF 027
Resources	Logic elements (LEs)	573,480	764,640	1,178,525	1,437,240	1,918,975	2,308,080	2,208,075	2,692,760
	Adaptive logic modules (ALMs)	194,400	259,200	399,500	487,200	650,500	782,400	748,500	912,800
	ALM registers	777,600	1,036,800	1,598,000	1,948,800	2,602,000	3,129,600	2,994,000	3,651,200
	High-performance crypto blocks	0	0	0	0	2	2	0	0
	eSRAM memory blocks	0	0	2	2	1	1	0	0
	eSRAM memory size (Mb)	0	0	36	36	18	18	0	0
	M20K memory blocks	2,844	3,792	5,900	7,110	8,500	10,464	10,900	13,272
	M20K memory size (Mb)	56	74	115	139	166	204	212	259
	MLAB memory count	9,720	12,960	19,975	24,360	32,525	39,120	37,425	45,640
	MLAB memory size (Mb)	6	8	12	15	20	24	23	28
	Fabric PLL	6	6	8	8	5	5	12	12
	I/O PLL	12	12	16	16	10	10	16	16
	Variable-precision digital signal processing (DSP) blocks	1,640	2,296	3,743	4,510	1,354	1,640	6,250	8,528
	18 x 19 multipliers	3,280	4,592	7,486	9,020	2,708	3,280	12,500	17,056
	Single-precision or half-precision tera floating point operations per second (TFLOPS)	2.5 / 5.0	3.5 / 6.9	6.0 / 12.0	6.8 / 13.6	2.0 / 4.0	2.5 / 5.0	9.4 / 18.8	12.8 / 25.6
	Maximum EMIF x72[2]	4	4	4	4	3	3	4	4
Maximum Available Device Resources	Maximum differential (RX or TX) pairs	192	288	384	384	240	240	384	384
	Maximum AIB interfaces	2	2	2	2	4	4	4	4
	Memory devices supported	DDR4 and QDR IV							
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support							
	Hard processor system	Quad-core 64 bit Arm Cortex*-A53 up to 1.50 GHz with 32 KB I/D cache, Neon* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4							
Tile Resources	F-Tile	PCI Express* (PCIe*) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 GbE hard IP block (10/25/50/100/200 Gbps FEC/PCS) IEEE 1588 v2 support PMA direct							
	E-Tile	Transceiver channel count : Up to 24 channels at 28.9 Gbps (NRZ) / 12 channels at 57.8 Gbps (PAM4) - RS & KP FEC[1] Networking support : - 400GbE (4 x 100GbE hard IP blocks (10/25 GbE FEC/PCS/MAC)) IEEE 1588 v2 support PMA direct							
	P-Tile	PCIe hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) SR-IOV 8PF / 2kVF VirtIO support Scalable IOV							

F- Tile - Package Options and I/O Pins	GPIO (LVDS) / F-Tile 32G NRZ (58G PAM4)							
1546A (F-Tile x2) (37.5 mm x 34 mm, 0.92 mm Hex)	384(192)/32(24)	384(192)/32(24)						
2340A (F-Tile x2) (45 mm x 42 mm, 0.92 mm Hex)	576(288)/32(24)	576(288)/32(24)	744(372)/32(24)	744(372)/32(24)	480(240)/32(24)	480(240)/32(24)	744(372)/32(24)	744(372)/32(24)
2340A (F-Tile x1) (45 mm x 42 mm, 0.92 mm Hex)	576(288)/16(12)	576(288)/16(12)	744(372)/16(12)	744(372)/16(12)				
3184C (F-Tile x4) (56 mm x 45 mm, 0.92 mm Hex)					480(240)/64(48)	480(240)/64(48)	720(360)/64(48)	720(360)/64(48)

E-Tile and P-Tile - Package Options and I/O Pins	GPIO (LVDS) / E-Tile 28.9G NRZ (57.8G PAM4) / P-Tile 16G PCIe							
2486A (E-Tile x1 & P-Tile x1) (55 mm x 42.5 mm, 1.0 mm Hex)			768(384)/16(8)/16	768(384)/16(8)/16				
2581A (E-Tile x1 & P-Tile x2) (50 mm x 40.5 mm, 0.92/0.94 mm Hex)[3]					480(240)/24(12)/32	480(240)/24(12)/32	624/(312)/24(12)/32	624(312)/24(12)/32

Notes:
1. Only 4 instances of KP-FEC are supported when using 100GE MAC.
2. Max EMIF count achieved using AVST x8 mode Compact - Address/Cmd lane [3 lanes] configuration.
3. Conditional migration path from AGF 019/023 to AGF 022/027 devices.
4. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

Devices: Intel Agilex FPGA Portfolio

Intel Agilex 7 FPGA and SoC I-Series Features

View device ordering codes on page 55.

Product Line		AGI 019	AGI 023	AGI 022	AGI 027	AGI 035	AGI 040	AGI 041
Resources	Logic elements (LEs)	1,918,975	2,308,080	2,208,075	2,692,760	3,540,000	4,047,400	4,000,672
	Adaptive logic modules (ALMs)	650,500	782,400	748,500	912,800	1,200,000	1,372,000	1,356,160
	ALM registers	2,602,000	3,129,600	2,994,000	3,651,200	4,800,000	5,488,000	5,424,640
	High-performance crypto blocks	2	2	0	0	4	4	4
	eSRAM memory blocks	1	1	0	0	3	3	2
	eSRAM memory size (Mb)	18	18	0	0	54	54	36
	M20K memory blocks	8,500	10,464	10,900	13,272	14,931	19,908	17,136
	M20K memory size (Mb)	166	204	212	259	292	389	335
	MLAB memory count	32,525	39,120	37,425	45,640	60,000	68,600	67,808
	MLAB memory size (Mb)	20	24	23	28	37	42	42
	Fabric PLL	5	5	12	12	6	6	8
	I/O PLL	10	10	16	16	12	12	16
	Variable-precision digital signal processing (DSP) blocks	1,354	1,640	6,250	8,528	9,594	12,792	0
	18 x 19 multipliers	2,708	3,280	12,500	17,056	19,188	25,584	0
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	2.4 / 4.9	2.4 / 4.9	9.4 / 18.8	12.8 / 25.6	14.3 / 28.7	19.1 / 38.3	0
Maximum Available Device Resources	Maximum EMIF x72[1]	3	3	4	4	4	4	4
	Maximum differential (RX or TX) pairs	240	240	360	360	288	288	372
	Maximum AIB Interfaces	4	4	4	4	6	6	4
	Memory devices supported	DDR4 and QDR IV						
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support						
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache , Neon coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4				n/a		HPS support[2]
Tile Resources	F-Tile	PCIe hard IP block (4.0 x16) or Bifurcateable 2x PCIe 4.0 x8 (EP) or 4x 4.0 x4 (RP) Transceiver channel count : - 4 channels at 116 Gbps (PAM4) / 58 Gbps (NRZ) - 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) IEEE 1588 support PMA direct						
	R-Tile	CXL - Link width x16 lanes, x8 lanes PCIe hard IP block (5.0 x16) or Bifurcateable 2x PCIe 5.0 x8 (EP) or 4x 5.0 x4 (RP) Virtualization (SR-IOV) supporting 8 PFs/2k VFs Scalable IOV VirtIO support Precise time management PIPE direct						

F-Tile - Package Options and I/O Pins	Tile Configuration	GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) Channels						
3184B (56 mm x 45 mm, 0.92 mm Hex)	F-Tile x4	480(240)/64(48)/8(8)	480(240)/64(48)/8(8)	720(360)/64(48)/8(8)	720(360)/64(48)/8(8)			732(366)/64(48)/8(8)
3948A (56mm x 56mm, 0.92 mm Hex)	F-Tile x6					576(288)/96(72)/24(24)	576(288)/96(72)/24(24)	
F-Tile and R-Tile - Package Options and I/O Pins	**Tile Configuration**	**GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ(116G PAM4) Channels / R- Tile 32G PCIe (CXL) Lanes**						
1805A (42.5mm x 42.5mm, 1.025 mm Hex)	F-Tile x1 & R-Tile x 1	480(240)/16(12)/0(0)/16(16)	480(240)/16(12)/0(0)/16(16)					
2957A[3] (56 mm x 45 mm, 1.0 / 0.92 mm Hex)	F-Tile x1 & R-Tile x 3			720(360)/16(12)/4(4)/48(32)	720(360)/16(12)/4(4)/48(32)			720(360)/16(12)/4(4)/48(32)
3184A (56 mm x 45 mm, 0.92 mm Hex)	F Tile x3 & R-Tile x1			720(360)/48(36)/8(8)/16(16)	720(360)/48(36)/8(8)/16(16)			
3184E (56 mm x 45 mm, 0.92 mm Hex)	F Tile x2 & R-Tile x2							744(372)/32(24)/8(8)/32(32)

Notes:
1. Max EMIF count achieved using AVST x8 mode Compact - Address/Cmd lane [3 lanes] configuration
2. Same HPS as AGI 027/022/023/019
3. Conditional pin migration from AGI 022/027 to AGI 041 device.
4. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

Intel Agilex 7 FPGA and SoC M-Series Features

View device ordering codes on page 55.

Product Line		AGM 032	AGM 039
Resources	Logic elements (LEs)	3,245,000	3,851,520
	Adaptive logic modules (ALMs)	1,100,000	1,305,600
	ALM registers	4,400,000	5,222,400
	M20K memory blocks	15,932	18,960
	M20K memory size (Mb)	311	370
	MLAB memory count	55,000	65,280
	MLAB memory size (Mb)	33	40
	High-bandwidth DRAM memory size (HBM2E) (Gigabytes)	16 / 32	16 / 32
	Fabric PLL	8	8
	I/O PLL	16	16
	Variable-precision digital signal processing (DSP) blocks	9,375	12,300
	18 x 19 multipliers	18,750	24,600
	Single-precision or half-precision tera floating point operations per second (TFLOPS)	14 / 28	18.4 / 37
	Maximum EMIF x72	4	4
Maximum Available Device Resources	Memory devices supported	LPDDR5, DDR5, DDR4	
	Maximum AIB interfaces	4	
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support	
	Hard processor system	Quad-core 64 bit Arm Cortex-A53 up to 1.41GHz with 32KB I/D cache, Neon coprocessor, 1 MB L2 Cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general prupose timers x7, watchdog timer x4	
Tile Resources	F-Tile	PCIe hard IP block (4.0 x16) or bifurcateable 2x PCIe 4.0 x8 (EP) or 4x 4.0 x4 (RP) Transciever channel count : - 4 channels at 116 Gbps (PAM4) / 58 Gbps (NRZ) - 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) IEEE 1588 support PMA direct	
	R-Tile	CXL - Link width x16 lanes, x8 lanes PCIe hard IP block (5.0 x16) or Bifurcateable 2x PCIe 5.0 x8 (EP) or 4x 5.0 x4 (RP) Virtualization (SR-IOV) supporting 8 PFs/2k VFs Scalable IOV VirtIO Support Precise Time Management PIPE Direct	

Product Line	AGM 032	AGM 039
Package Options (HBM2E Packages)	GPIO (LVDS) / F-Tile 32G NRZ (58G PAM4) / High-Speed Transceiver58G NRZ (116G PAM4) / R- Tile 32G PCIe (CXL) Lanes	
4700A (F-Tile x3, R-Tile x1, HBM2E) (56 mm x 66 mm, 0.92 mm Hex)	768(384) / 48(36) / 8(8) / 16(16)	768(384) / 48(36) / 8(8) / 16(16)
4700B (F-Tile x4, HBM2E) (56 mm x 66 mm, 0.92 mm Hex)	768(384) / 64(48) / 8(8)	768(384) / 64(48) / 8(8)

Product Line	AGM 032	AGM 039
Package Options (Non-HBM2E Packages)	GPIO (LVDS) / F-Tile 32G NRZ (58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4)/ R- Tile 32G PCIe (CXL) Lanes	
3184B (F-Tile x4) (56 mm x 45 mm, 0.92 mm Hex)	720(360) / 64(48) / 8(8)	720(360) / 64(48) / 8(8)

Note:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

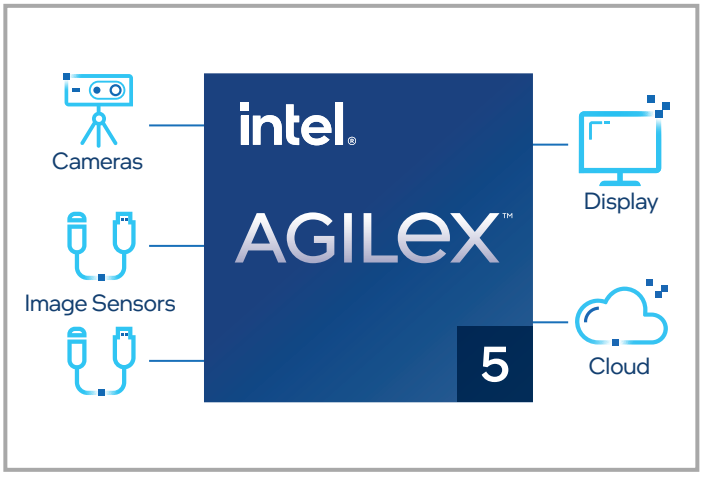
Intel Agilex 5 FPGA and SoC Overview

Intel Agilex 5 Devices

Intel Agilex 5 devices serve a broad range of applications that require high performance, lower power, and smaller form factors. This tier consists of the performance-optimized D-Series FPGAs and the power-optimized E-Series FPGAs. Intel Agilex 5 devices also feature the industry's first Enhanced DSP with AI Tensor Block, which deliver high-efficiency AI and digital signal processing (DSP) functionality, and the FPGA industry's first asymmetric applications processor system consisting of dual Arm Cortex-A76 cores and dual Cortex-A55 cores, which enable you to optimize the performance and power efficiency of their workloads. These characteristics make them ideal for midrange FPGA applications across the edge and core including wireless and wireline communications, video and broadcast equipment, industrial applications, test and measurement products, medical electronics, and defense applications.

E-Series FPGAs and SoCs	D-Series FPGAs and SoCs
E-Series FPGAs and SoCs are optimized for power and size— with 50% lower power while delivering up to 2.5X better performance as compared to Cyclone V devices, also with features including transceiver rates up to 24x28 Gbps, PCIe 4.0x4, 6x25GbE, 3,600 Mbps DDR5, dual-core Arm Cortex-A76 and dual-core Cortex-A5 processors make it ideal for intelligent applications at the edge, embedded, and more.	D-Series FPGAs and SoCs are optimized for performance and power efficiency— with 42% lower power while delivering up to 1.5X better performance as compared to Intel Stratix 10 FPGAs, also with features including transceiver rates up to 32x28 Gbps, PCIe 4.0x8, 16x25GbE, 4,000 Mbps DDR5, dual-core Cortex-A76 and dual-core Cortex-A55 processors make it deal for various applications across multiple markets.

Image Sensor Processing

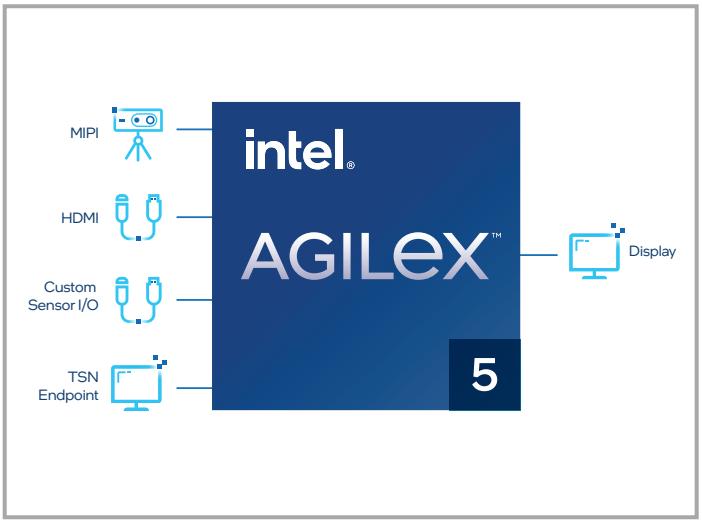


Inline image processing
- Pixel defect correction
- Vignette correction
- Adaptive noise reduction

Customized Connectivity
- High-definition multimedia interface (HDMI)
- MIPI D-PHY

Hard Processor System
- Flexible embedded software stack
- Graphical user interface

Autonomous Mobile Robots



Flexible I/O

- MIPI
- HDMI
- Time-Sensitive Networking (TSN)
- LVDS

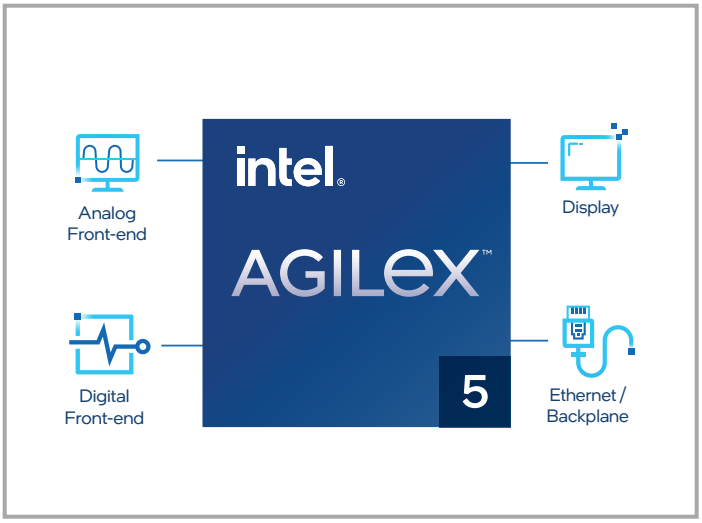
FPGA Acceleration

- Sensor fusion
- Point of cloud processing

Hard Processor System

- RTOS
- Hypervisor functions
- Network features
- User application

Clinical System



Power Optimized

- Low-density option
- Battery-powered clinical equipment

FPGA Acceleration

- Custom image progressing
- AR/VR innovations
- Deterministic low latency

Hard Processor System

- Real-time waveform analysis
- Graphic controls for Human-Machine Interaction (HMI)

Intel Agilex 5 FPGA and SoC E-Series Features

Product Line		Device Group A FPGAs				
		A5E 013A	A5E 028A	A5E 043A	A5E 052A	A5E 065A
Resources	Logic elements (LEs)	138,060	282,256	434,240	523,920	656,080
	Adaptive logic modules (ALMs)	46,800	95,680	147,200	177,600	222,400
	ALM registers	187,200	382,720	588,800	710,400	889,600
	M20K memory blocks	358	716	1,050	1,288	1,611
	M20K memory size (Mb)	6.99	13.98	20.51	25.16	31.46
	MLAB memory count	2,340	4,784	6,720	8,440	11,120
	MLAB memory size (Mb)	1.43	2.92	4.10	5.15	6.79
	I/O PLL	4	4	8	8	8
	Fabric-feeding I/O PLL[1]	8	10	13	13	13
	Variable-precision digital signal processing (DSP) blocks	188	376	564	676	846
	18 x 19 multipliers	376	752	1,128	1,352	1,692
	Peak INT8 (TOPS)	5.78	11.55	17.33	20.78	25.99
Maximum Available Device Resources	LVDS pairs at 1.6 Gbps	96	96	192	192	192
	DDR4/5 and LPDDR4/5 interfaces (x32)	2	2	4	4	4
	MIPI D-PHY interface	14	14	28	28	28
	Differential (RX or TX) pairs at 28 Gbps	4	12	16	24	24
	PCIe 4.0 x4 instance	1	3	4	6	6
	High-speed I/O (HSIO)	192	192	384	384	384
	High-voltage I/O (HVIO)	200	200	120	120	120
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support				
	Hard processor system	Multi-core with 32-bit/64-bit dual-core Arm Cortex-A55 up to 1.5 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.8 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2.				
	Transceiver	PCIe hard IP up to PCIe 4.0 x4 EP and RP Transceiver channel count: up to 24 channels at 28 Gbps (NRZ) Ethernet IP: up to 6 x10/25 GbE hard IP (MAC, PCS, and FEC)				

Package Options[2] and I/O Pins

Package code (Package size, ball pitch, grid array pattern)	HVIO/ HSIO/Transceivers				
B23A (23 mm x 23 mm, Variable[3, 4], Variable Pitch BGA)	120/96/4	120/96/12	120/96/12	120/96/12	120/96/12
B32A (32 mm x 32 mm, Variable[3, 4], Variable Pitch BGA)	200/192/4	200/192/12	120/384/16	120/384/24	120/384/24

Notes:
1. The fabric-feeding IOPLL count inclusive of system PLL at transceiver bank, the System PLL can be repurposed for core fabric usage if not used for transceiver.
2. For more information about the device migration path, please refer to the AN 979: Agilex 5 FPGAs and SoCs Device Migration Guidelines: E-Series Application Note.
3. The ball pitch is variable, from 0.65mm - 1.45mm to ease signal routing. Please contact your sales representative for more details.
4. VPBGA packaging uses Type III PCB with the same design rules as 0.8mm ball pitch and standard plated through hole (PTH) vias.
5. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

Product Line		Device Group B FPGAs							
		A5E 005B	A5E 007B	A5E 008B	A5E 013B	A5E 028B	A5E 043B	A5E 052B	A5E 065B
Resources	Logic elements (LEs)	50,445	69,030	85,196	138,060	282,256	434,240	523,920	656,080
	Adaptive logic modules (ALMs)	17,100	23,400	28,880	46,800	95,680	147,200	177,600	222,400
	ALM registers	68,400	93,600	115,520	187,200	382,720	588,800	710,400	889,600
	M20K memory blocks	130	179	229	358	716	1,050	1,288	1,611
	M20K memory size (Mb)	2.54	3.50	4.47	6.99	13.98	20.51	25.16	31.46
	MLAB memory count	850	1,170	1,780	2,340	4,784	6,720	8,440	11,120
	MLAB memory size (Mb)	0.52	0.71	1.09	1.43	2.92	4.10	5.13	6.79
	I/O PLL	2	2	4	4	4	8	8	8
	Fabric-feeding I/O PLL[1]	5	5	8	8	10	13	13	13
	Variable-precision digital signal processing (DSP) blocks	65	94	116	188	376	564	676	846
	18 x 19 multipliers	130	188	232	376	752	1,128	1,352	1,692
	Peak INT8 (TOPS)	1.7	2.46	3.05	4.93	9.85	14.78	17.72	22.17
Maximum Available Device Resources	LVDS pairs at 1,250 Mbps	48	48	96	96	96	192	192	192
	DDR4 and LPDDR4/5 interfaces (x32)	1	1	2	2	2	4	4	4
	MIPI D-PHY interface	7	7	14	14	14	28	28	28
	Differential (RX or TX) pairs at 17 Gbps	0	0	4	4	12	16	24	24
	PCIe 4.0 x4 instance	0	0	1	1	3	4	6	6
	High-speed I/O (HSIO)	96	96	192	192	192	384	384	384
	High-voltage I/O (HVIO)	160	160	200	200	200	120	120	120
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support							
	Hard processor system	NA		Multi-core with 32-bit/64-bit dual-core Arm Cortex-A55 up to 1.33 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.6 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2.					
	Transceiver	NA		PCIe hard IP up to PCIe 4.0 x4 EP and RP Transceiver channel count: up to 24 channels at 17 Gbps (NRZ) Ethernet IP: up to 6 x10 GbE hard IP (MAC, PCS, and FEC)					

Package Options[2] and I/O Pins

Package code (Package size, ball pitch, grid array pattern)	HVIO/ HSIO/Transceivers							
B15A (15 mm x 15 mm, Variable[3, 4], Variable Pitch BGA)	80/62	80/62						
M16A (16 mm x 16 mm, 0.5 mm, Standard BGA)			40/192/4	40/192/4	40/192/8			
B18A (18mm x 18mm, Variable[3, 4], Variable Pitch BGA)	160/48	160/48						
B23B (23 mm x 23 mm, Variable[3, 4], Variable Pitch BGA)	160/96	160/96	160/192	160/192	160/192			
B23A (23 mm x 23 mm, Variable[3, 4], Variable Pitch BGA)			120/96/4	120/96/4	120/96/12	120/96/12	120/96/12	120/96/12
B32A (32 mm x 32 mm, Variable[3, 4], Variable Pitch BGA)			200/192/4	200/192/4	200/192/12	120/384/16	120/384/24	120/384/24

Notes:
1. The fabric-feeding IOPLL count inclusive of system PLL at transceiver bank, the System PLL can be repurposed for core fabric usage if not used for transceiver.
2. For more information about the device migration path, please refer to the AN 979: Agilex 5 FPGAs and SoCs Device Migration Guidelines: E-Series Application Note.
3. The ball pitch is variable, from 0.65mm - 1.45mm to ease signal routing. Please contact your sales representative for more details.
4. VPBGA packaging uses Type III PCB with the same design rules as 0.8mm ball pitch and standard plated through hole (PTH) vias.
5. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

Intel Agilex 5 FPGA and SoC D-Series Features

Product Line		A5D 010	A5D 025	A5D 031	A5D 051	A5D 064
Resources	Logic elements (LEs)	103,250	254,054	318,600	515,070	644,280
	Adaptive logic modules (ALMs)	35,000	86,120	108,000	174,600	218,400
	ALM registers	140,000	344,480	432,000	698,400	873,600
	M20K memory blocks	534	1,281	1602,	2,563	3,204
	M20K memory size (Mb)	10.43	25.02	31.29	50.06	62.58
	MLAB memory count	1780	3420	5,400	8,440	10,920
	MLAB memory size (Mb)	1.09	2.09	3.30	5.15	6.67
	I/O PLL	8	8	8	8	8
	Fabric-feeding I/O PLL[1]	11	11	11	15	15
	Variable-precision digital signal processing (DSP) blocks	276	736	920	1,472	1,840
	18 x 19 multipliers	552	1,472	1,840	2,944	3,680
	Peak INT8 (TOPS)	8.48	22.61	28.26	45.22	56.22
Maximum Available Device Resources	LVDS pairs at 1.6 Gbps	192	192	192	192	192
	DDR4 interface (x64)	2	2	2	2	2
	DDR4/5 and LPDDR4/5 interfaces (x32)	4	4	4	4	4
	MIPI D-PHY interface	28	28	28	28	28
	Differential (RX or TX) pairs at 28 Gbps	16	16	16	24	32
	PCIe 4.0 x4 instance	4	4	4	6	8
	PCIe 4.0 x8 instance	2	2	2	3	4
	High-speed I/O (HSIO)	384	384	384	384	384
	High-voltage I/O (HVIO)	60	60	60	60	60
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support				
	Hard processor system	Multi-core with 32-bit/64-bit dual-core Arm Cortex-A55 up to 1.5 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.8 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2.				
	Transceiver	PCIe hard IP up to PCIe 4.0 x8 EP and RP Transceiver channel count: up to 32 channels at 28 Gbps (NRZ) Ethernet IP: up to 16 x10/25 GbE hard IP (MAC, PCS, and FEC)				

Package Options and I/O Pins

Package code (Package size, ball pitch, grid array pattern)	HVIO/ HSIO/Transceivers				
B23A (23 mm x 23 mm, Variable[2, 3], Variable Pitch BGA)	60/192/8	60/192/8	60/192/8		
B32A (32 mm x 32 mm, Variable[2, 3], Variable Pitch BGA)	60/384/16	60/384/16	60/384/16	60/384/24	60/384/32

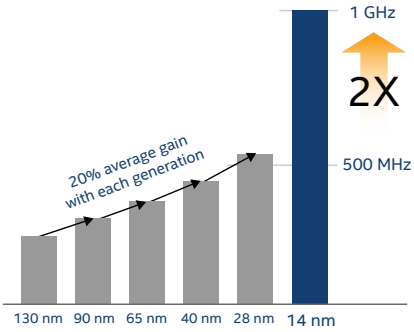
Note:
1. The fabric-feeding IOPLL count inclusive of system PLL at transceiver bank, the System PLL can be repurposed for core fabric usage if not used for transceiver.
2. The ball pitch is variable, from 0.65mm - 1.45mm to ease signal routing. Please contact your sales representative for more details.
3. VPBGA packaging uses Type III PCB with the same design rules as 0.8mm ball pitch and standard plated through hole (PTH) vias.
4. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

Generation 10 FPGAs and SoCs

Intel's Generation 10 FPGAs and SoCs are optimized based on process technology and architecture to deliver the industry's highest performance and highest levels of system integration at the lowest power. Generation 10 device families include Intel Stratix 10 FPGAs and SoCs, Intel Arria 10 FPGAs and SoCs, Intel Cyclone 10 FPGAs, and Intel MAX 10 FPGAs.

Intel® Stratix® 10

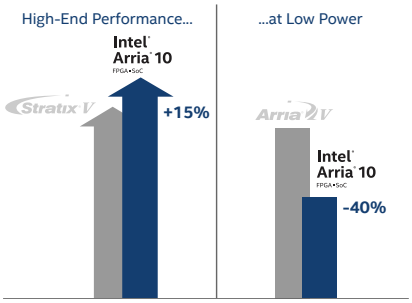
FPGA ▪ SoC



- 2X core performance with revolutionary Intel Hyperflex® FPGA Architecture†
- Up to 70% power savings†
- Highest density FPGA with up to 10.2 M logic elements (LEs)
- 64 bit quad-core Arm Cortex-A53 processor system
- Up to 10 tera floating point operations per second (TFLOPS) single-precision floating-point throughput
- Built on Intel's 14 nm Tri-Gate process technology

Intel® Arria® 10

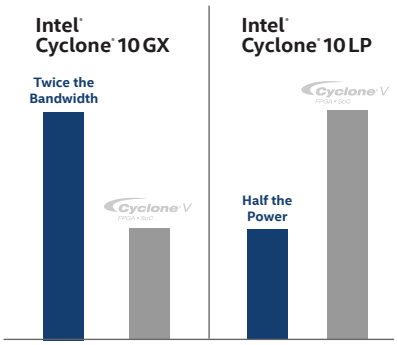
FPGA ▪ SoC



- 15% higher performance than the previous high-end devices†
- 40% lower midrange power†
- 1.5 GHz dual-core Arm Cortex-A9 processor
- IP core support, including 100G Ethernet, 150G/300G Interlaken, and PCI Express 3.0
- Built on TSMC's 20 nm process technology

Intel® Cyclone® 10

FPGA



Intel Cyclone 10 GX

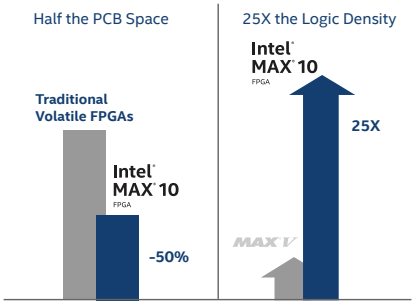
- Optimized for high-bandwidth, high-performance applications
- The industry's first low-cost FPGA with 12.5 Gbps transceiver I/O support
- High-performance 1,866 Mbps external memory interface
- 1.434 Gbps LVDS I/Os
- The industry's first low-cost FPGA with IEEE 754 compliant hard floating-point DSP blocks

Intel Cyclone 10 LP

- Optimized for cost and power-sensitive applications
- Chip-to-chip bridging
- I/O expansion
- Control applications

Intel® MAX® 10

FPGA



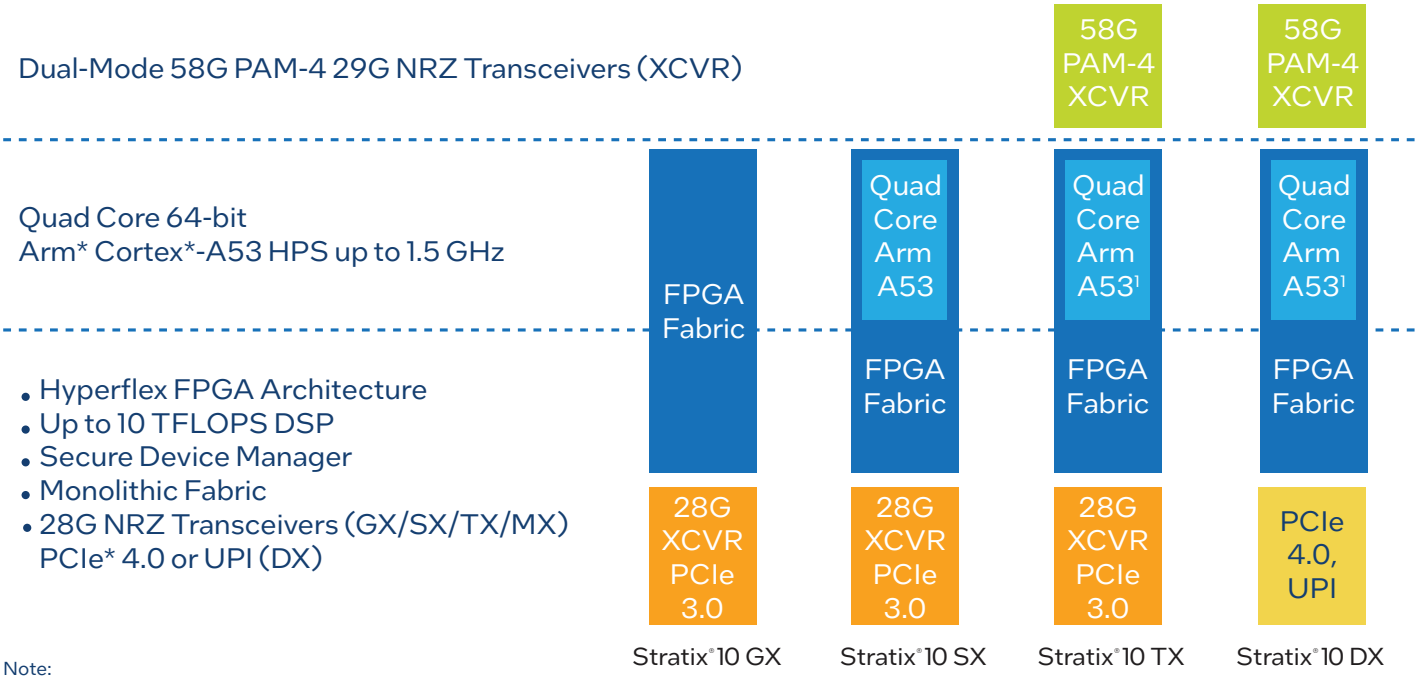
- Single-chip, dual-configuration non-volatile FPGA
- Optimal system component integration for half the PCB space of traditional volatile FPGAs
- Broad range of IP including analog-to-digital converters (ADCs), DSP, and the Nios II embedded soft processor

Intel Stratix 10 FPGA and SoC Overview

intel.com/stratix10

Intel FPGAs and SoCs deliver breakthrough advantages in performance, power efficiency, density, and system integration that are unmatched in the industry. Featuring the revolutionary Intel Hyperflex FPGA Architecture and built on the Intel 14 nm Tri-Gate process, Intel Stratix 10 devices deliver 2X core performance gains over previous-generation, high-performance FPGAs with up to 70% lower power†.

Stratix® 10 Device Family Variants



Note:
1. Not available in every device.

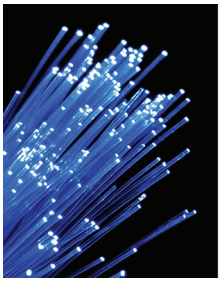
The figure above shows the core performance benchmarks achieved by early access customers using the Intel Stratix 10 Hyperflex FPGA architecture. With the 2X performance increase, customers in multiple end markets can achieve significant improvements in both throughput and area utilization, with up to 70% lower power†.

Intel Stratix 10 FPGA and SoC system integration breakthroughs include:

- Heterogeneous 3D system in package (SiP) integration
- The highest density FPGA fabric with up to 10.2 million LEs
- Up to 10 TFLOPS of IEEE 754 compliant single-precision floating-point DSP throughput
- Secure Device Manager (SDM) with the most comprehensive security capabilities
- Integrated quad-core 64 bit Arm Cortex-A53 hard processor system up to 1.5 GHz
- Dual-mode 28.9 Gbps non-return-to-zero (NRZ) and 57.8 Gbps PAM-4 transceivers

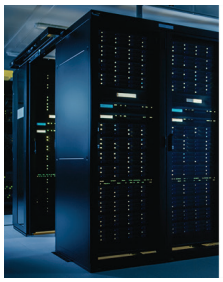
These unprecedented capabilities make Intel Stratix 10 devices uniquely positioned to address the design challenges in next-generation, high-performance systems in virtually all end markets including wireline and wireless communications, computing, storage, military, broadcast, medical, and test and measurement.

Communications



- 400G/500G/1T optical transmission
- 200G/400G bridging and aggregation
- 982 MHz remote radio head
- Mobile backhaul
- 5G wireless communications

Computing and Storage

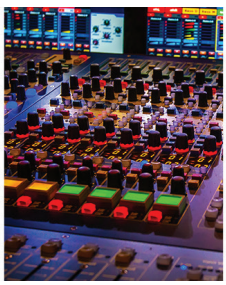


- Data center server acceleration
- High-performance computing (HPC)
- Oil and gas exploration
- Bioscience

Defense

- Next-generation radar
- Secure communications
- Avionics and guidance systems

Broadcast



- High-end broadcast studio
- High-end broadcast distribution
- Headend encoder or EdgeQAM or converged multiservice access platform (CMAP)

Devices: Generation 10 Device Portfolio

Intel Stratix 10 GX FPGA Features

View device ordering codes on page 56.

	Product Line	GX 400	GX 650	GX 850	GX 1100	GX 1650	GX 2100	GX 2500	GX 2800	GX 1660	GX 2110	GX 10M
Resources	Logic elements (LEs)[1]	378,000	612,000	841,000	1,325,000	1,624,000	2,005,000	2,422,000	2,753,000	1,679,000	2,073,000	10,200,000
	Adaptive logic modules (ALMs)	128,160	207,360	284,960	449,280	550,540	679,680	821,150	933,120	569,200	702,720	3,466,080
	ALM registers	512,640	829,440	1,139,840	1,797,120	2,202,160	2,718,720	3,284,600	3,732,480	2,276,800	2,810,880	13,864,320
	Hyper-Registers from Intel Hyperflex FPGA Architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric										
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees										
	M20K memory blocks	1,537	2,489	3,477	5,461	5,851	6,501	9,963	11,721	6,162	6,847	12,950
	M20K memory size (Mb)	30	49	68	107	114	127	195	229	120	134	253
	MLAB memory size (Mb)	2	3	4	7	8	11	13	15	9	11	55
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,592	3,145	3,744	5,011	5,760	3,326	3,960	3,456
	18 x 19 multipliers	1,296	2,304	4,032	5,184	6,290	7,488	10,022	11,520	6,652	7,920	6,912
	Peak fixed-point performance (TMACS)[2]	2.6	4.6	8.1	10.4	12.6	15.0	20.0	23.0	13.3	15.8	13.8
	Peak floating-point performance (TFLOPS)[3]	1.0	1.8	3.2	4.1	5.0	6.0	8.0	9.2	5.3	6.3	5.5
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side-channel attack protection										–
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4								–	–	–
	Maximum user I/O pins	374	392	688	688	704	704	1160	1160	688	688	2,304
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	120	192	336	336	336	336	576	576	336	336	1152[5]
	Total full duplex transceiver count	24	24	48	48	96	96	96	96	48	48	48
	GXT full duplex transceiver count (up to 28.3 Gbps)	16	16	32	32	64	64	64	64	32	32	–
	GX full duplex transceiver count (up to 17.4 Gbps)	8	8	16	16	32	32	32	32	16	16	48
	PCI Express hard intellectual property (IP) blocks (3.0 x16)	1	1	2	2	4	4	4	4	2	2	4[6]
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys										

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[7,8]

F1152 pin (35 mm x 35 mm, 1.0 mm pitch)	374,56,120,24	392,8,192,24	–	–	–	–	–	–	–	–	
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)	–	–	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)	–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96	–	–	
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)	–	–	–	–	–	–	1160,8,576,24	1160,8,576,24	–	–	
F4938 pin (70 mm x 74 mm, 1.0 mm pitch)											2304, 32, 1152, 48

Notes:
1. LE counts valid in comparing across Intel FPGAs, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system only available in Intel Stratix 10 SX SoCs.
5. 1.4 Gbps LVDS maximum rate for GX 10M.
6. PCIe 3.0 x 8 support for GX 10M.
7. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
8. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

392,8,192,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration path.

Intel FPGA Product Catalog

Devices: Generation 10 Device Portfolio

Intel Stratix 10 TX FPGA Features

View device ordering codes on page 56.

	Product Line	TX 400	TX 850	TX 850	TX 1100	TX 1100	TX 1650	TX 2100	TX 2500	TX 2500	TX 2800	TX 2800
Resources	Logic elements (LEs)[1]	378,000	841,000	841,000	1,325,000	1,325,000	1,679,000	2,073,000	2,422,000	2,422,000	2,753,000	2,753,000
	Adaptive logic modules (ALMs)	128,160	284,960	284,960	449,280	449,280	569,200	702,720	821,150	821,150	933,120	933,120
	ALM registers	512,640	1,139,840	1,139,840	1,797,120	1,797,120	2,276,800	2,810,880	3,284,600	3,284,600	3,732,480	3,732,480
	Hyper-Registers from Intel Hyperflex FPGA Architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric										
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees										
	eSRAM memory blocks	–	–	–	–	–	2	2	–	–	–	–
	eSRAM memory size (Mb)	–	–	–	–	–	94.5	94.5	–	–	–	–
	M20K memory blocks	1,537	3,477	3,477	5,461	5,461	6,162	6,847	9,963	9,963	11,721	11,721
	M20K memory size (Mb)	30	68	68	107	107	120	134	195	195	229	229
	MLAB memory size (Mb)	2	4	4	7	7	9	11	13	13	15	15
	Variable-precision digital signal processing (DSP) blocks	648	2,016	2,016	2,592	2,592	3,326	3,960	5,011	5,011	5,760	5,760
	18 x 19 multipliers	1,296	4,032	4,032	5,184	5,184	6,652	7,920	10,022	10,022	11,520	11,520
	Peak fixed-point performance (TMACS)[2]	2.6	8.1	8.1	10.4	10.4	13.3	15.8	20.0	20.0	23.0	23.0
	Peak floating-point performance (TFLOPS)[3]	1.0	3.2	3.2	4.1	4.1	5.3	6.3	8.0	8.0	9.2	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side-channel attack protection										
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4										
		Yes	Yes	Yes	Yes	Yes	–	–	Yes	Yes	Yes	Yes
	Maximum user I/O pins	384	440	440	440	440	440	440	440	296	440	296
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	144	216	216	216	216	216	216	216	144	216	144
	Total full duplex transceiver count	24	48	72	48	72	96	96	96	144	96	144
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	12 PAM-4 24 NRZ	12 PAM-4 24 NRZ	24 PAM-4 48 NRZ	12 PAM-4 24 NRZ	24 PAM-4 48 NRZ	36 PAM-4 72 NRZ	36 PAM-4 72 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ	36 PAM-4 72 NRZ	60 PAM-4 120 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	0	16	16	16	16	16	16	16	16	16	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	0	8	8	8	8	8	8	8	8	8	8
	PCI Express hard intellectual property (IP) blocks (3.0 x16)	0	1	1	1	1	1	1	1	1	1	1
	100G Ethernet MAC (no FEC) hard IP blocks	0	1	1	1	1	1	1	1	1	1	1
	100G Ethernet MAC + FEC hard IP blocks	4	4	8	4	8	12	12	12	20	12	20
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys										

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, E-Tile Transceiver Count and H-Tile Transceiver Count[5,6]

F1152 pin (35mm x 35mm, 1.0mm pitch)	384,0,144,24,0										
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		440,8,216,24,24	–	440,8,216,24,24	–	–	–	–	–	–	–
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)	–	–	440,8,216,48,24	–	440,8,216,48,24	440,8,216,72,24	440,8,216,72,24	440,8,216,72,24	–	440,8,216,72,24	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)	–	–	–	–	–	–	–	–	296,8,144,120,24	–	296,8,144,120,24

Notes:
1. LE counts valid in comparing across Intel FPGAs, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system present in select Intel Stratix 10 TX devices.
5. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
6. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

296,8,144,120,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, GXE (E-Tile) transceiver count, and GXT+GX (H-Tile) transceiver count

Indicates pin migration path.

Product Line	Hard Processor System (HPS)
Processor	Quad-core 64 bit Arm Cortex-A53 MPCore processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • Arm NEON media engine • Arm CoreSight debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4 and DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA
USB On-The-Go (OTG) controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
Serial peripheral interface (SPI) controller	4X SPI
I²C controller	5X I²C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	4X
Software-programmable general-purpose I/Os (GPIOs)	Maximum 48 GPIOs
HPS DDR Shared I/Os	3X 48 - May be assigned to HPS for HPS DDR access
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitstream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side-channel attack protection

Notes:
1. With overdrive feature.

Intel FPGA Product Catalog

Devices: Generation 10 Device Portfolio

Intel Stratix 10 DX FPGA Features

View device ordering codes on page 57.

	Product Line	DX 1100	DX 2800
Resources	Logic elements (LEs)[1]	1,325,000	2,753,000
	Adaptive logic modules (ALMs)	449,280	933,120
	ALM registers	1,797,120	3,732,480
	Hyper-Registers from Intel Hyperflex FPGA Architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric	
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees	
	M20K memory blocks	5,461	11,721
	M20K memory size (Mb)	107	229
	MLAB memory size (Mb)	7	15
	Variable-precision digital signal processing (DSP) blocks	2,592	5,760
	18 x 19 multipliers	5,184	11,520
	Peak fixed-point performance (TMACS)[2]	10.4	23.0
	Peak floating-point performance (TFLOPS)[3]	4.1	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side-channel attack protection	
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4	
		Yes	–
	Maximum user I/O pins	528	816
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	264	408
	Total full duplex transceiver count - non return to zero (NRZ)	32	84
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	8 PAM-4, or 16 NRZ	4 PAM-4, or 8 NRZ
	GXP transceiver count - NRZ (up to 16 Gbps)	16	76
	UPI/PCI Express 4.0 x16 hard intellectual property (IP) blocks (configurable for UPI or PCIe operation)	-	3
	PCI Express 4.0 x16 hard IP blocks (supports PCIe only)	1	1
	100G Ethernet media access control (MAC) + forward error correction (FEC) hard IP blocks	4	2
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3	
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, P-Tile Transceiver Count and E-Tile Transceiver Count			
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		528,0,264,16,16	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	816,0,408,76,8

Notes:
1. LE counts valid in comparing across Intel FPGAs, and are conservative vs. competing FPGAs.
2. Fixed-point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system present in select Intel Stratix 10 DX devices.
5. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

816,0,408,76,8 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, P-Tile transceiver count, E-Tile transceiver count.

Product Line	Hard Processor System (HPS)
Processor	Quad-core 64 bit Arm Cortex-A53 MPCore processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • Arm NEON media engine • Arm CoreSight debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4, DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA
USB On-The-Go (OTG) controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
Serial peripheral interface (SPI) controller	4X SPI
I^2C controller	5X I^2C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	4X
Software-programmable general-purpose I/Os (GPIOs)	Maximum 48 GPIOs
HPS DDR Shared I/Os	3X 48 - May be assigned to HPS for HPS DDR access
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitstream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side-channel attack protection

Notes:
1. With overdrive feature.

Devices: Generation 10 Device Portfolio

Intel Stratix 10 SX SoC Features

View device ordering codes on page 56.

	Product Line	SX 400	SX 650	SX 850	SX 1100	SX 1650	SX 2100	SX 2500	SX 2800
Resources	Logic elements (LEs)[1]	378,000	612,000	841,000	1,325,000	1,624,000	2,005,000	2,422,000	2,753,000
	Adaptive logic modules (ALMs)	128,160	207,360	284,960	449,280	550,540	679,680	821,150	933,120
	ALM registers	512,640	829,440	1,139,840	1,797,120	2,202,160	2,718,720	3,284,600	3,732,480
	Hyper-Registers from Intel Hyperflex FPGA Architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric							
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees							
	M20K memory blocks	1,537	2,489	3,477	5,461	5,851	6,501	9,963	11,721
	M20K memory size (Mb)	30	49	68	107	114	127	195	229
	MLAB memory size (Mb)	2	3	4	7	8	11	13	15
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,592	3,145	3,744	5,011	5,760
	18 x 19 multipliers	1,296	2,304	4,032	5,184	6,290	7,488	10,022	11,520
	Peak fixed-point performance (TMACS)[2]	2.6	4.6	8.1	10.4	12.6	15.0	20.0	23.0
	Peak floating-point performance (TFLOPS)[3]	1.0	1.8	3.2	4.1	5.0	6.0	8.0	9.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side-channel attack protection							
	Hard processor system[4]	Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4							
	Maximum user I/O pins	374	392	688	688	704	704	1160	1160
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	120	192	336	336	336	336	576	576
	Total full duplex transceiver count	24	24	48	48	96	96	96	96
	GXT full duplex transceiver count (up to 28.3 Gbps)	16	16	32	32	64	64	64	64
	GX full duplex transceiver count (up to 17.4 Gbps)	8	8	16	16	32	32	32	32
	PCI Express hard intellectual property (IP) blocks (3.0 x16)	1	1	2	2	4	4	4	4
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys							

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[5,6]

	SX 400	SX 650	SX 850	SX 1100	SX 1650	SX 2100	SX 2500	SX 2800
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)	374,56,120,24	392,8,192,24	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)	–	–	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)	–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)	–	–	–	–	–	–	1160,8,576,24	1160,8,576,24

Notes:
1. LE counts valid in comparing across Intel FPGAs, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system only available in Intel Stratix 10 SX SoCs.
5. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
6. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

392,8,192,24 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

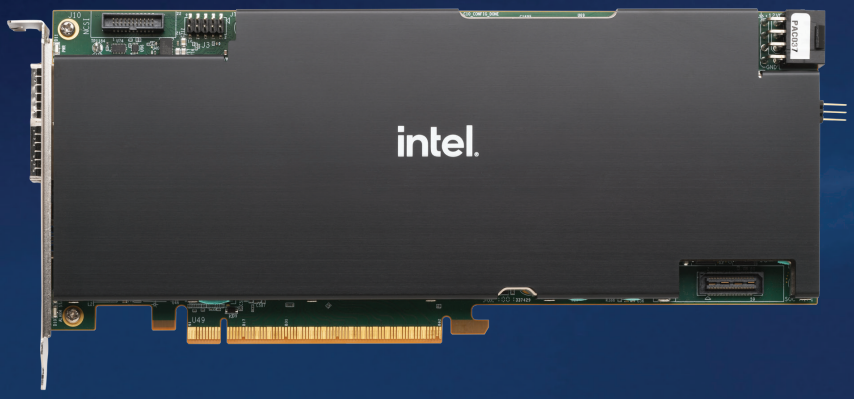
Indicates pin migration path.

Product Line	Hard Processor System (HPS)
Processor	Quad-core 64 bit Arm Cortex-A53 MPCore processor
Maximum processor frequency	1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) with error correction code (ECC) • Level 2 cache (1 MB) with ECC • Floating-point unit (FPU) single and double precision • Arm NEON media engine • Arm CoreSight debug and trace technology • System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4 and DDR3 (Up to 64 bit with ECC)
Direct memory access (DMA) controller	8 channels
EMAC	3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA
USB On-The-Go (OTG) controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
Serial peripheral interface (SPI) controller	4X SPI
I²C controller	5X I²C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	4X
Software-programmable general-purpose I/Os (GPIOs)	Maximum 48 GPIOs
HPS DDR Shared I/O	3X 48 - May be assigned to HPS for HPS DDR access
Direct I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitstream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side-channel attack protection

Notes:
1. With overdrive feature.

Accelerator Cards That Fit Your Performance Needs

Intel® FPGA-based acceleration solutions make it possible to move, process, and store data faster and more efficiently. Intel and partner Infrastructure Processing Units (IPUs), SmartNICs, and acceleration platforms offer hardware programmability on production-qualified cards, which enable the quick design and deployment of workloads in networking, wireless, cloud, and data center applications.



Artiza Networks Griffin SmartNIC N6060/N6061

BittWare IA-220-U2

BittWare IA-420F

BittWare IA-840F

BittWare IA-440i

BittWare IA-780i

BittWare IA-820i

BittWare IA-821i

BittWare IA-860m

BittWare IA-865m

CAES APD Vortex

EmbedWay PA8921

Flyslice FA728Q

Flyslice FA927S

Flyslice FA925E

Hitek HiPrAcc CS200D

Hitek HiPrAcc NC100

Hitek HiPrAcc NC200

Hitek HiPrAcc NCS200

Inventec FPGA IPU C5020X

Napatech F2070X IPU

Prodesign FALCON

Ruijie C5040X

Silicom FPGA IPU C5010X

Silicom FPGA SmartNIC N5013/ N5014

Silicom FPGA SmartNIC N6010/N6011

Terasic DE10-Agilex

WNC FPGA SmartNIC WSN6050/6051

For more information, please visit:
www.intel.com/content/www/us/en/products/details/fpga/platforms.html

Intel Arria 10 FPGA and SoC Overview

intel.com/arria10

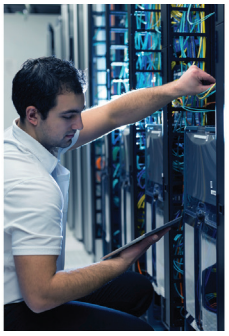
Intel Arria 10 FPGAs and SoCs deliver the highest performance at 20 nm, offering a one speed-grade performance advantage over competing devices. Intel Arria 10 FPGAs and SoCs are up to 40% lower power than previous generation FPGAs and SoCs, and feature the industry's only hard floating-point DSP blocks with speeds up to 1,500 giga floating-point operations per second (GFLOPS)†. The Intel Arria 10 FPGAs and SoCs are ideal for the following end market applications.

Wireless

Applications

- Remote radio head
- Mobile backhaul
- Active antenna
- Base station
- 4G/Long Term Evolution (LTE) macro eNB
- Wideband Code Division Multiple Access (W-CDMA)

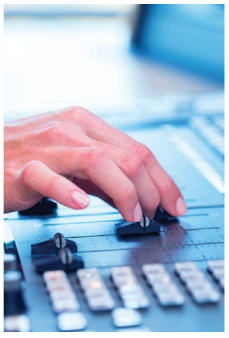
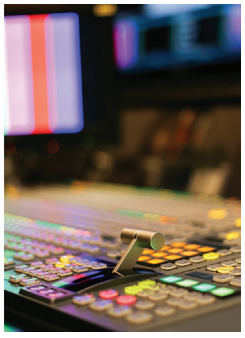
Cloud Service and Storage



Applications

- Flash cache
- Cloud
- Server
- Financial
- Bioscience
- Oil and gas
- Data center server acceleration

Broadcast

Applications

- Switcher
- Server
- Encoder/decoder
- Capture cards
- Editing
- Monitors
- Multiviewers

Devices: Generation 10 Device Portfolio

Intel Arria 10 FPGA Features

View device ordering codes on page 57.

Product Line		GX 160	GX 220	GX 270	GX 320	GX 480	GX 570	GX 660	GX 900	GX 1150	GT 900	GT 1150
Resources	Part number reference	10AX016	10AX022	10AX027	10AX032	10AX048	10AX057	10AX066	10AX090	10AX115	10AT090	10AT115
	LEs (K)	160	220	270	320	480	570	660	900	1,150	900	1,150
	System logic elements (K)	210	288	354	419	629	747	865	1,180	1,506	1,180	1,506
	Adaptive logic modules (ALMs)	61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200	339,620	427,200
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800	1,358,480	1,708,800
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133	2,423	2,713	2,423	2,713
	M20K memory (Mb)	9	11	15	17	28	35	42	47	53	47	53
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7	9.2	12.7	9.2	12.7
	Hardened single-precision floating-point multipliers/ adders	156/156	192/192	830/830	985/985	1,368/1,368	1,523/1,523	1,687/1,687	1,518/1,518	1,518/1,518	1,518/1,518	1,518/1,518
	18 x 19 multipliers	312	384	1,660	1,970	2,736	3,046	3,374	3,036	3,036	3,036	3,036
	Peak fixed-point performance (GMACS)[1]	343	420	1,826	2,167	3,010	3,351	3,714	3,340	3,340	3,340	3,340
	Peak floating-point performance (GFLOPS)	140	172	747	887	1,231	1,371	1,519	1,366	1,366	1,366	1,366
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16	16	16	16	16
	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0										
	I/O standards supported	3 V I/O pins only: 3 V LVTTL, 2.5 V CMOS DDR and LVDS I/O pins: POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL All I/Os: 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-135, SSTL-125, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-135, Differential SSTL-125, Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12										
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	324	270	384	384	312	312
	Maximum user I/O pins	288	288	384	384	492	696	696	768	768	624	624
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48	96	96	72	72
	Transceiver count (25.78 Gbps)	–	–	–	–	–	–	–	–	–	6	6
	PCI Express hardened IP blocks (3.0 x8)	1	1	2	2	2	2	2	4	4	4	4
	Maximum 3 V I/O pins	48	48	48	48	48	48	48	–	–	–	–
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC										

Package Options[2] and I/O Pins[3]: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs[4], and Transceiver Count

U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72,6	–	–	–	–	–	–	–	–	–
F27	F672 pin (27 mm)	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	–	–	–	–	–	–	–
F29	F780 pin (29 mm)	288, 48, 120, 12	288, 48, 120, 12	360, 48, 156, 12	360, 48, 156, 12	360, 48, 156, 12	–	–	–	–	–	–
F34	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	492, 48, 222, 24	492, 48, 222, 24	492, 48, 222, 24	504, 0, 252, 24	504, 0, 252, 24	–	–
F35	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	396, 48, 174, 36	396, 48, 174, 36	396, 48, 174, 36	–	–	–	–
KF40	F1517 pin (40 mm)	–	–	–	–	–	696, 96, 324, 36	696, 96, 324, 36	–	–	–	–
NF40	F1517 pin (40 mm)	–	–	–	–	–	588, 48, 270, 48	588, 48, 270, 48	600, 0, 300, 48	600, 0, 300, 48	–	–
RF40	F1517 pin (40 mm)	–	–	–	–	–	–	–	342, 0, 154, 66	342, 0, 154, 66	–	–
NF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	768, 0, 384, 48	768, 0, 384, 48	–	–
SF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	624, 0, 312, 72	624, 0, 312, 72	624, 0, 312, 72	624, 0, 312, 72
UF45	F1932 pin (45 mm)	–	–	–	–	–	–	–	480, 0, 240, 96	480, 0, 240, 96	–	–

Notes:
1. Fixed-point performance assumes the use of pre-adders.
2. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
3. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
4. Each LVDS pair can be configured as either a differential input or a differential output.
5. Certain packages might not bond out all PCI Express hard IP blocks.
6. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

192, 48, 72, 6 — Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration.

Intel FPGA Product Catalog

Devices: Generation 10 Device Portfolio

Intel Arria 10 SoC Features

View device ordering codes on page 57.

Product Line		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Resources	Part number reference	10AS016	10AS022	10AS027	10AS032	10AS048	10AS057	10AS066
	LEs (K)	160	220	270	320	480	570	660
	System Logic Elements (K)	210	288	354	419	629	747	865
	ALMs	61,510	83,730	101,620	118,730	181,790	217,080	250,540
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133
	M20K memory (Mb)	9	11	15	17	28	35	42
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7
	Hardened single-precision floating-point multipliers/ adders	156/156	192/192	830/830	985/985	1,368/1,368	1,523/1,523	1,687/1,687
	18 x 19 multipliers	312	1687/1687	1,660	1,970	2,736	3,046	3,374
	Peak fixed-point performance (GMACS)[1]	343	420	1,826	2,167	3,010	3,351	3,714
	Peak floating-point performance (GFLOPS)	140	172	747	887	1,231	1,371	1,519
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16
	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0						
	I/O standards supported	3 V I/O pins only: 3 V LVTTL, 2.5 V CMOS DDR and LVDS I/O pins: POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL All I/Os: 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-135, SSTL-125, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-135, Differential SSTL-125, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	270	270
	Maximum user I/O pins	288	288	384	384	492	696	696
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48
	Transceiver count (25.78 Gbps)	–	–	–	–	–	–	–
	PCI Express hardened IP blocks (3.0 x8)	1	1	2	2	2	2	2
	Maximum 3 V I/O pins	48	48	48	48	48	48	48
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II						

Package Options[2] and I/O Pins[3]: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs[4], and Transceiver Count

U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72,6	–	–	–	–	–
F27	F672 pin (27 mm)	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96, 12	–	–	–
F29	F780 pin (29 mm)	288, 48, 120, 12	288, 48, 120, 12	360, 48, 156, 12	360, 48, 156, 12	360, 48, 156, 12	–	–
F34	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	492, 48, 222, 24	492, 48, 222, 24	492, 48, 222, 24
F35	F1152 pin (35 mm)	–	–	384, 48, 168, 24	384, 48, 168, 24	396, 48, 174, 36	396, 48, 174, 36	396, 48, 174, 36
KF40	F1517 pin (40 mm)	–	–	–	–	–	696, 96, 324, 36	696, 96, 324, 36
NF40	F1517 pin (40 mm)	–	–	–	–	–	588, 48, 270, 48	588, 48, 270, 48

Notes:
1. Fixed-point performance assumes the use of pre-adders.
2. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
3. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
4. Each LVDS pair can be configured as either a differential input or a differential output.
5. Certain packages might not bond out all PCI Express hard IP blocks.
6. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

192, 48, 72, 6 Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration.

Product Line	Hard Processor System (HPS)
Processor	Dual-core Arm Cortex-A9 MPCore processor
Maximum processor frequency	1.2 -1.5 GHz[1]
Processor cache and co-processors	• L1 instruction cache (32 KB) • L1 data cache (32 KB) • Level 2 cache (512 KB) shared • FPU single and double precision • Arm Neon media engine • Arm CoreSight debug and trace technology • Snoop control unit (SCU) • Acceleration coherency port (ACP)
Scratch pad RAM	256 KB
HPS DDR memory	DDR4 and DDR3 (Up to 64 bit with ECC)
DMA controller	8 channels
EMAC	3X 10/100/1000 EMAC with integrated DMA
USB OTG controller	2X USB OTG with integrated DMA
UART controller	2X UART 16550 compatible
SPI controller	4X SPI
I^2C controller	5X I^2C
Quad SPI flash controller	1X SIO, DIO, QIO SPI flash supported
SD/SDIO/MMC controller	1X eMMC 4.5 with DMA and CE-ATA support
NAND flash controller	• 1X ONFI 1.0 or later • 8 and 16 bit support
General-purpose timers	7X
Software-programmable GPIOs	Maximum 54 GPIOs
Direct shared I/Os	48 I/Os to connect HPS peripherals directly to I/O
Watchdog timers	4X
Security	Secure boot, AES, and secure hash algorithm

Notes:
1. With overdrive feature.

Intel FPGA Product Catalog

Intel Cyclone 10 FPGA Overview

intel.com/cyclone10

Intel Cyclone 10 FPGAs deliver cost and power savings over previous generations of Intel Cyclone FPGAs. Intel Cyclone 10 GX FPGAs provide high bandwidth via 12.5G transceiver-based functions, 1.4 Gbps LVDS, and 1,866 Mbps DDR3 SDRAM, and feature a hard floating-point DSP block in a low-cost FPGA. Intel Cyclone 10 LP devices offer low static power, cost-optimized functions.

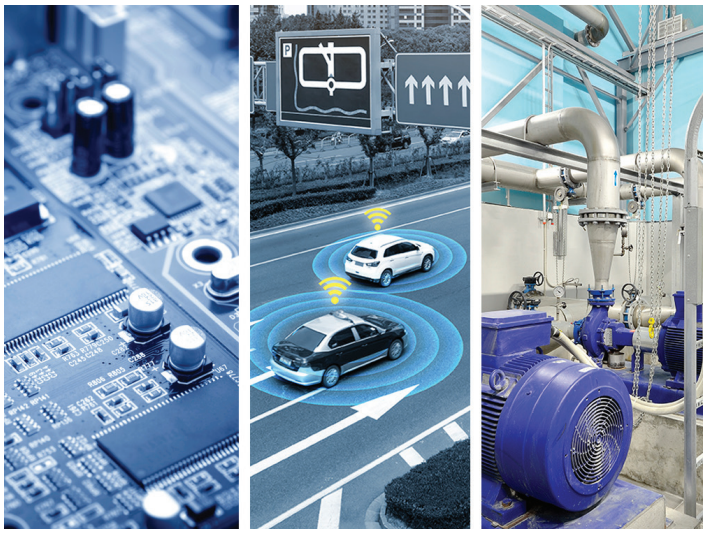
- Intel Cyclone 10 GX FPGAs are optimized for high bandwidth‡
- Intel Cyclone 10 LP FPGAs are optimized for power and cost-sensitive applications

Intel Cyclone 10 GX FPGA

- Low-cost 12.5 Gbps transceivers
- 1,866 Mbps 72 bit DDR3 SDRAM interface
- 1.4 Gbps LVDS
- The industry's first low-cost FPGA with hard floating-point blocks

GX Applications

- Embedded vision cameras
- Industrial robotics
- Machine vision
- Programmable logic controllers
- Pro-AV systems



Intel Cyclone 10 LP FPGA

- Designed for power-sensitive applications
- Simplified core power supply requirements
- High I/O count to package density ratio
- Embedded Nios II soft processor support

LP Applications

- I/O expansion
- Interfacing
- Chip-to-chip bridging
- Sensor fusion
- Industrial motor control

‡ Compared to previous generation Cyclone FPGAs, cost comparisons are based on list price. Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

Intel Cyclone 10 GX FPGA Features

View device ordering codes on page 58.

	Product Line	10CX085	10CX105	10CX150	10CX220
Resources	Logic elements (LEs)[1]	85,000	104,000	150,000	220,000
	Adaptive logic modules (ALMs)	31,000	38,000	54,770	80,330
	ALM registers	124,000	152,000	219,080	321,320
	M20K memory blocks	291	382	475	587
	M20K memory size (Kb)	5,820	7,640	9,500	11,740
	MLAB memory size (Kb)	653	799	1,152	1,690
	Variable-precision digital signal processing (DSP) blocks	84	125	156	192
	18 x 19 multipliers	168	250	312	384
	Peak fixed-point performance (GMACS)[2]	151	225	281	346
	Peak floating-point performance (GFLOPS)[3]	59	88	109	134
I/O and Architectural Features	Global clock networks	32	32	32	32
	Regional clocks	8	8	8	8
	Maximum user I/O pins	192	284	284	284
	Maximum LVDS pairs 1.4 Gbps (RX or TX)	72	118	118	118
	Maximum transceiver count (12.5 Gbps)	6	12	12	12
	Maximum 3V I/O pins	48	48	48	48
	PCI Express hard IP blocks (2.0 x4)[4]	1	1	1	1
	Memory devices supported	DDR3, DDR3L, LPDDR3			

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, 3V I/O Count, LVDS Pairs, Total Transceiver count[5]

U484 pin (19 mm x 19 mm, 0.8 mm pitch)	188, 48, 70, 6	188, 48, 70, 6	188, 48, 70, 6	188, 48, 70, 6
F672 pin (27 mm x 27 mm, 1.0 mm pitch)	192, 48, 72, 6	236, 48, 94, 10	236, 48, 94, 10	236, 48, 94, 10
F780 pin (29 mm x 29 mm, 1.0 mm pitch)		284, 48, 118, 12	284, 48, 118, 12	284, 48, 118, 12

Notes:
1. LE counts valid in comparing across Intel FPGAs, and are conservative versus competing FPGAs.
2. Fixed-point performance assumes the use of pre-adders.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Hard PCI Express IP core x2 in U484 package
5. Each LVDS pair can be configured as either a differential input or differential output.
6. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
7. All data is correct at the time of printing and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

284,48,118,12 Numbers indicate GPIO count, 3V I/O count, LVDS pairs, total transceiver count.

Indicates pin migration path.

Devices: Generation 10 Device Portfolio

Cyclone 10 LP FPGA Features

View device ordering codes on page 58.

Product Line		10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
Resources	Logic elements (LEs)[1]	6,000	10,000	16,000	25,000	40,000	55,000	80,000	120,000
	M9K memory blocks	30	46	56	66	126	260	305	432
	M9K memory size (Kb)	270	414	504	594	1,134	2,340	2,745	3,888
	DSP blocks (18 x 18 multipliers)	15	23	56	66	126	156	244	288
	Phase-locked loops (PLL)	2	2	4	4	4	4	4	4
I/O and Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	Maximum user I/O pins	176	176	340	150	325	321	423	525
	Maximum LVDS channels	65	65	137	52	124	132	178	230
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, LVDS Pairs[2]									
E144 pin (22 mm x 22mm, 0.5 mm pitch)		88, 22	88, 22	78, 19	76, 18				
M164 pin (8 mm x 8 mm, 0.5 mm pitch)			101,26	87, 22					
U256 pin (14 mm x 14 mm, 0.8 mm pitch)		176, 65	176, 65	162, 53	150, 52				
U484 pin (19 mm x 19 mm, 0.8 mm pitch)				340, 137		325, 124	321, 132	289, 110	
F484 pin (23 mm x 23 mm, 1.0 mm pitch)				340, 137		325, 124	321, 132	289, 110	277, 103
F780 pin (29 mm x 29 mm, 1.0 mm pitch)								423, 178	525, 230

Notes:
1. LE counts valid in comparing across Intel FPGAs, and are conservative versus competing FPGAs.
2. This includes both dedicated and emulated LVDS pairs
3. All data is correct at the time of printing and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

88, 22 Numbers indicate GPIO count, LVDS pairs.

Indicates pin migration path.

Intel MAX 10 FPGA Overview

intel.com/max10

Intel MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor, programmable logic device.

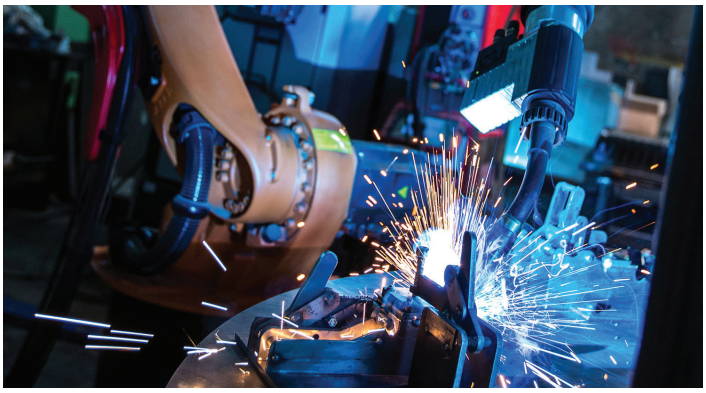
Intel MAX 10 FPGAs are built on TSMC's 55 nm flash technology, enabling instant-on configuration so you can quickly control the power-up or initialization of other components in the system. The devices also include full-featured FPGA capabilities, such as DSP, analog functionality, Nios II Gen2 embedded soft processor support, and memory controllers.

With a robust set of FPGA capabilities, Intel MAX 10 FPGAs are optimized for a wide range of high-volume, cost-sensitive applications, including:

Automotive

- Built on TSMC's 55 nm high-volume flash process tailored for the automotive industry's rigorous safety and quality requirements
- Integrated flash provides instant-on behavior for applications requiring fast boot times such as rear-view cameras in advanced driver assistance systems (ADAS) and infotainment displays
- FPGA-class signal processing acceleration for electric vehicle (EV) applications, such as motor control, battery management, and power conversion

Industrial



- Reduced footprint, increased design security and reliability, and lower system cost
- Accurate environmental condition sensing and efficient real-time controls for motor control, I/O modules, and Internet of Things (IoT) applications
- Single-chip support for multiple industrial Ethernet protocols and machine-to-machine (M2M) communication

Communications

- Analog functionality for sensing board environment allows integration of power-up sequencing and system-monitoring circuitry in a single device
- High I/O count and software-based system management using the Nios II soft processor enable board management integration in an advanced, reliable, single-chip system controller

Intel MAX 10 FPGA Features

View device ordering codes on page 58.

Product Line	10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)	2	4	8	16	25	40	50
Block memory (Kb)	108	189	378	549	675	1,260	1,638
User flash memory[1] (KB)	12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers	16	20	24	45	55	125	144
PLLs[2]	1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration	Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD)[3]	-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)	Yes[4]	Yes[4]	Yes[4]	Yes[5]	Yes[5]	Yes[5]	Yes[5]

Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transmitter[9]/Receiver[9]

V36 (D)[6]	WLCSP (3 mm, 0.4 mm pitch)	C, 27, 3/10	–	–	–	–	–	–
V81 (S)	WLCSP (4 mm, 0.4 mm pitch)			L, 58, 7/25				
V81 (D)[7]	WLCSP (4 mm, 0.4 mm pitch)	–	–	C/F, 56, 7/25	–	–	–	–
Y180 (S)	WLCSP (6x5 mm, 0.35 mm pitch)				L, 125, 10/53			
E144 (S)[6]	EQFP (22 mm, 0.5 mm pitch)	C, 101, 7/45	C/A, 101, 10/41	C/A, 101, 10/41	C/A, 101, 10/41	C/A, 101, 10/41	C/A, 101, 10/42	C/A, 101, 10/42
M153 (S)	MBGA (8 mm, 0.5 mm pitch)[8]	C, 112, 9/49	C/A, 112, 9/49	C/A, 112, 9/49	–	–	–	–
U169 (S)	UBGA (11 mm, 0.8 mm pitch)	C, 130, 9/58	C/A, 130, 9/58	C/A, 130, 9/58	C/A, 130, 9/58	–	–	–
U324 (S)	UBGA (15 mm, 0.8 mm pitch)	C, 246, 15/114	C/A, 246, 15/114	C/A, 246, 15/114	C/A, 246, 15/114			
U324 (D)	UBGA (15 mm, 0.8 mm pitch)	C, 160, 9/73	C/A, 246, 15/114	C/A, 246, 15/114	C/A, 246, 15/114	–	–	–
F256 (D)	FBGA (17 mm, 1.0 mm pitch)	–	C/A, 178, 13/80	C/A, 178, 13/80	C/A, 178, 13/80	C/A, 178, 13/80	C/A, 178, 13/80	C/A, 178, 13/80
F484 (D)	FBGA (23 mm, 1.0 mm pitch)	–	–	C/A, 250, 15/116	C/A, 320, 22/151	C/A, 360, 24/171	C/A, 360, 24/171	C/A, 360, 24/171
F672 (D)	FBGA (27 mm, 1.0 mm pitch)	–	–	–	–	–	C/A, 500, 30/241	C/A, 500, 30/241

Notes:
1. Additional user flash may be available, depending on configuration options.
2. The number of PLLs available is dependent on the package option.
3. Availability of the ADC or TSD varies by package type. Smaller pin-count packages do not have access to the ADC hard IP.
4. SRAM only.
5. SRAM, DDR3 SDRAM, DDR2 SDRAM, or LPDDR2.
6. "D" = Dual power supply (1.2 V/2.5 V), "S" = Single power supply (3.3 V or 3.0 V).
7. V81 package does not support analog feature set. 10M08 V81 F devices support dual image with RSU.
8. "Easy PCB" utilizes 0.8 mm PCB design rules.
9. Some LVDS channels at bottom bank can be configured as TX or RX, refer to the Intel MAX 10 High-Speed LVDS I/O User Guide for details.
10. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

C, 27, 3/10 — Indicates feature set options, GPIO count, and LVDS transmitter or receiver count. Feature set options: C = Compact (single image), F/L = Flash (dual image with RSU), A = Analog (analog features block). Each has added premiums.

Indicates pin migration.

Devices: 28 nm Device Portfolio

Arria V FPGA and SoC Features

View device ordering codes on page 59.

Product Line		Arria V GX FPGAs[1]								Arria V GT FPGAs[1]				Arria V GZ FPGAs[1]				Arria V SX SoCs[1]		Arria V ST SoCs[1]	
		5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7	5AGTC3	5AGTC7	5AGTD3	5AGTD7	5AGZE1	5AGZE3	5AGZE5	5AGZE7	5ASXB3	5ASXB5	5ASTD3	5ASTD5
Resources	LEs (K)	75	156	190	242	300	362	420	504	156	242	362	504	220	360	400	450	350	462	350	462
	ALMs	28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240	58,900	91,680	136,880	190,240	83,020	135,840	150,960	169,800	132,075	174,340	132,075	174,340
	Registers	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960	235,600	366,720	547,520	760,960	332,080	543,360	603,840	679,200	528,300	697,360	528,300	697,360
	M10K memory blocks	800	1,051	1,180	1,366	1,510	1,726	2,054	2,414	1,051	1,366	1,726	2,414	–	–	–	–	1,729	2,282	1,729	2,282
	M20K memory blocks	–	–	–	–	–	–	–	–	–	–	–	–	585	957	1,440	1,700	–	–	–	–
	M10K memory (Kb)	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140	10,510	13,660	17,260	24,140	–	–	–	–	17,290	22,820	17,290	22,820
	M20K memory (Kb)	–	–	–	–	–	–	–	–	–	–	–	–	11,700	19,140	28,800	34,000	–	–	–	–
	MLAB memory (Kb)	463	961	1,173	1,448	1,852	2,098	2,532	2,906	961	1,448	2,098	2,906	2,594	4,245	4,718	5,306	2,014	2,658	2,014	2,658
	Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,156	396	800	1,045	1,156	800	1,044	1,092	1,139	809	1,090	809	1,090
	18 x 18 multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,312	792	1,600	2,090	2,312	1,600	2,088	2,184	2,278	1,618	2,180	1,618	2,180
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (Arm Cortex-A9)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (GHz)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1.05[2]	1.05[2]	1.05[2]	1.05[2]
	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[3] (FPGA)	10	10	12	12	12	12	16	16	10	12	12	16	20	20	24	24	14	14	14	14
	PLLs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	3	3	3
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[4]																			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																			
	Maximum LVDS pairs (receiver/transmitter)	80/67	80/67	136/120	136/120	176/160	176/160	176/160	176/160	80/68	136/120	176/160	176/160	108/99	108/99	168/166	168/166	136/120	136/120	136/120	136/120
	Transceiver count (6.5536 Gbps)	9	9	24	24	24	24	36	36	3	6	6	6	–	–	–	–	30	30	30	30
	Transceiver count (10.3125 Gbps)[5]	–	–	–	–	–	–	–	–	4	12	12	20	–	–	–	–	–	–	16	16
	Transceiver count (12.5 Gbps)	–	–	–	–	–	–	–	–	–	–	–	–	24	24	36	36	–	–	–	–
	PCI Express hardened IP blocks (2.0 x4)	1	1	2	2	2	2	2	2	1	2	2	2	–	–	–	–	2	2	2	2
	PCI Express hardened IP blocks (2.0 x8, 3.0)	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1	–	–	–	–
	GPIOs (FPGA)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	540	540	540	540
	GPIOs (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	208	208	208	208
	Hard memory controllers[6] (FPGA)	2	2	4	4	4	4	4	4	2	4	4	4	–	–	–	–	3	3	3	3
	Hard memory controllers (HPS)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1
	Memory devices supported	DDR3, DDR2, DDR II+[7], QDR II, QDR II+, RLDRAM II, RLDRAM 3[8], LPDDR[7], LPDDR2[7]																			
Package Options and I/O Pins: GPIO Count, and Transceiver Count																					
F672 pin (27 mm, 1.0 mm pitch)		336 9,0	336 9,0	336 9,0	336 9,0	–	–	–	–	336 3,4	–	–	–	–	–	–	–	–	–	–	–
H780 pin (29 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	–	–	–	–	342 12	342 12	–	–	–	–		–
F896 pin (31 mm, 1.0 mm pitch)		416 9,0	416 9,0	384 18,0	384 18,0	384 18,0	384 18,0	–	–	416 3,4	384 6,8	384 6,8	–	–	–	–	–	250, 208 12+0	250, 208 12+0	250, 208 12+6	250, 208 12+6
F1152 pin (35 mm, 1.0 mm pitch)		–	–	544 24,0	544 24,0	544 24,0	544 24,0	544 24,0	544 24,0	–	544 6,12	544 6,12	544 6,12	414 24	414 24	534 24	534 24	385, 208 18+0	385, 208 18+0	385, 208 18+8	385, 208 18+8
F1517 pin (40 mm, 1.0 mm pitch)		–	–	–	–	704 24,0	704 24,0	704 36,0	704 36,0	–	–	704 6,12	704 6,20	–	–	674 36	674 36	540, 208 30+0	540, 208 30+0	540, 208 30+16	540, 208 30+16

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. 1.15 V operation.
3. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
4. For Arria V GZ devices, the I/O voltage of 3.3 V compliant, requires a 3.0 V power supply.
5. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels.
6. With 16 and 32 bit ECC support.
7. These memory interfaces are not available as Intel FPGA IP.
8. This memory interface is only available for Arria V GZ devices.

336 / 9,0 — For Arria V GX and GT devices, values on top indicate available user I/O pins and values at the bottom indicate the 6.5536 Gbps and 10.3125 Gbps transceiver count. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels. For Arria V GZ devices, values on top indicate available user I/O pins and values at the bottom indicate the 12.5 Gbps transceiver count.

250, 208 / 12+0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 6.5536 Gbps plus 10.3125 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labeled for pin migration.

Devices: 28 nm Device Portfolio

Cyclone V FPGA Features

View device ordering codes on page 60.

	Product Line	Cyclone V E FPGAs[1]					Cyclone V GX FPGAs[1]					Cyclone V GT FPGAs[1]		
		5CEA2	5CEA4	5CEA5	5CEA7	5CEA9	5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9	5CGTD5	5CGTD7	5CGTD9
Resources	LEs (K)	25	49	77	150	301	36	50	77	150	301	77	150	301
	ALMs	9,430	18,480	29,080	56,480	113,560	13,460	18,868	29,080	56,480	113,560	29,080	56,480	113,560
	Registers	37,736	73,920	116,320	225,920	454,240	53,840	75,440	116,320	225,920	454,240	116,320	225,920	454,240
	M10K memory blocks	176	308	446	686	1,220	135	250	446	686	1,220	446	686	1,220
	M10K memory (Kb)	1,760	3,080	4,460	6,860	12,200	1,350	2,500	4,460	6,860	12,200	4,460	6,860	12,200
	MLAB memory (Kb)	196	303	424	836	1,717	182	424	424	836	1,717	424	836	1,717
	Variable-precision DSP blocks	25	66	150	156	342	57	70	150	156	342	150	156	342
	18 x 18 multipliers	50	132	300	312	684	114	140	300	312	684	300	312	684
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	4	4	6	7	8	4	6	6	7	8	6	7	8
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3												
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS												
	Maximum LVDS pairs (receiver/transmitter)	56/56	56/56	60/60	120/120	120/120	52/52	84/84	84/84	120/120	140/140	84/84	120/120	140/140
	Transceiver count (3.125 Gbps)	–	–	–	–	–	3	6	6	9	12	–	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	–	–	6[4]	9[4]	12[4]
	PCI Express hardened IP blocks (1.0)[5]	–	–	–	–	–	1	2	2	2	2	–	–	–
	PCI Express hardened IP blocks (2.0)	–	–	–	–	–	–	–	–	–	–	2	2	2
	Hard memory controllers[6] (FPGA)	1	1	2	2	2	1	2	2	2	2	2	2	2
	Memory devices supported	DDR3, DDR2, LPDDR2												

Package Options and I/O Pins: GPIO Count, and Transceiver Count

M301 pin (11 mm, 0.5 mm pitch)							129 4	129 4				129 4		
M383 pin (13 mm, 0.5 mm pitch)	223	223	175				175 6	175 6				175 6		
M484 pin (15 mm, 0.5 mm pitch)				240					240 3				240 3	
U324 pin (15 mm, 0.8 mm pitch)	176	176				144 3								
U484 pin (19 mm, 0.8 mm pitch)	224	224	224	240	240	208 3	224 6	224 6	240 6	240 5		224 6	240 6	240 5
F256 pin (17 mm, 1.0 mm pitch)	128	128												
F484 pin (23 mm, 1.0 mm pitch)	224	224	240	240	224	208 3	240 6	240 6	240 6	224 6		240 6	240 6	224 6
F672 pin (27 mm, 1.0 mm pitch)				336	336		336 6	336 6	336 9	336 9		336 6	336 9	336 9
F896 pin (31 mm, 1.0 mm pitch)				480	480				480 9	480 12			480 9	480 12
F1152 pin (35 mm, 1.0 mm pitch)										560 12				560 12

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Automotive grade Cyclone V GT FPGAs include a 5 Gbps transceiver.
4. Transceiver counts shown are for ≤ 5 Gbps. The 6 Gbps channel count support depends on package and channel usage. Refer to Cyclone V Device Handbook Volume 2: Transceivers for guidelines.
5. Only one PCIe hard IP block supported in M301, M484, and U324 packages.
6. Includes 16 and 32 bit error correction code ECC support.

129 / 4 — Values on top indicate available user I/O pins; values at the bottom indicate the 3.125 Gbps, 5 Gbps, or 6.144 Gbps transceiver count.

Pin migration (same V_{CC}, GND, ISP, and input pins). User I/O pins may be less than labeled for pin migration.

For FPGAs: Pin migration is only possible if you use only up to 175 GPIOs.

Devices: 28 nm Device Portfolio

Cyclone V SoC Features

View device ordering codes on page 60.

	Product Line	Cyclone V SE SoCs[1]				Cyclone V SX SoCs[1]				Cyclone V ST SoCs[1]	
		5CSEA2	5CSEA4	5CSEA5	5CSEA6	5CSXC2	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
Resources	LEs (K)	25	40	85	110	25	40	85	110	85	110
	ALMs	9,430	15,880	32,070	41,910	9,430	15,880	32,070	41,910	32,070	41,910
	Registers	37,736	60,376	128,300	166,036	37,736	60,376	128,300	166,036	128,300	166,036
	M10K memory blocks	140	270	397	557	140	270	397	557	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570	1,400	2,700	3,970	5,570	3,970	5,570
	MLAB memory (Kb)	138	231	480	621	138	231	480	621	480	621
	Variable-precision DSP blocks	36	84	87	112	36	84	87	112	87	112
	18 x 18 multipliers	72	168	174	224	72	168	174	224	174	224
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (Arm Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual	Dual	Dual	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (MHz)	925	925	925	925	925	925	925	925	925	925
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	5	5	6	6	5	5	6	6	6	6
	PLLs (HPS)	3	3	3	3	3	3	3	3	3	3
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3									
	I/O standards supported	VTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS									
	Maximum LVDS pairs (receiver/transmitter)	37/32	37/32	72/72	72/72	37/32	37/32	72/72	72/72	72/72	72/72
	Transceiver count (3.125 Gbps)	–	–	–	–	6	6	9	9	–	–
	Transceiver count (6.144 Gbps)	–	–	–	–	–	–	–	–	9[3]	9[3]
	PCI Express hardened IP blocks (1.0)	–	–	–	–	2	2	2[4]	2[4]	–	–
	PCI Express hardened IP blocks (2.0)	–	–	–	–	–	–	–	–	2	2
	GPIOs (FPGA)	145	145	288	288	145	145	288	288	288	288
	GPIOs (HPS)	181	181	181	181	181	181	181	181	181	181
	Hard memory controllers[5] (FPGA)	1	1	1	1	1	1	1	1	1	1
	Hard memory controllers[5] (HPS)	1	1	1	1	1	1	1	1	1	1
	Memory devices supported	DDR3, DDR2, LPDDR2									

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, and Transceiver Count

U484 pin (19 mm, 0.8 mm pitch)	66, 151 0	66, 151 0	66, 151 0	66, 151 0						
U672 pin (23 mm, 0.8 mm pitch)	145, 181 0	145, 181 0	145, 181 0	145, 181 0	145, 181 6	145, 181 6	145, 181 6	145, 181 6		
F896 pin (31 mm, 1.0 mm pitch			288, 181 0	288, 181 0			288, 181 9	288, 181 9	288, 181 9	288, 181 9

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Transceiver counts shown are for ≤ 5 Gbps. The 6 Gbps channel count support depends on package and channel usage. Refer to Cyclone V Device Handbook Volume 2: Transceivers for guidelines.
4. One PCI Express hard IP block in U672 package.
5. With 16 and 32 bit ECC support.

66, 151 / 0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125 Gbps or 5 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labeled for pin migration.

For SoCs: Pin migration is only possible if you use only up to 138 GPIOs.

Devices: 60 nm Device Portfolio

Cyclone IV FPGA Features

View device ordering codes on page 61.

	Product Line	Cyclone IV GX FPGAs[1]							Cyclone IV E FPGAs[1]								
		EP4CGX15	EP4CGX22	EP4CGX30	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Resources	LEs (K)	14	21	29	50	74	109	150	6	10	15	22	29	40	56	75	114
	M9K memory blocks	60	84	120	278	462	666	720	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480	270	414	504	594	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	0	40	80	140	198	280	360	15	23	56	66	66	116	154	200	266
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	20	20	20/30	30	30	30	30	10	10	20	20	20	20	20	20	20
	PLLs	3	4	4/6	8	8	8	8	2	2	4	4	4	4	4	4	4
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3															
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12															
	Emulated LVDS channels	9	40	40	73	73	139	139	66	66	137	52	224	224	160	178	230
	Maximum LVDS pairs, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59	–	–	–	–	–	–	–	–	–
	Transceiver count[2] (2.5 Gbps/3.124 Gbps)	2/0	2, 0 / 4, 0	4, 0 / 0, 4[3]	0, 8	0, 8	0, 8	0, 8	–	–	–	–	–	–	–	–	–
	PCI Express hardened IP blocks (Base specification, Rev 1.1, 2.0, and so on)	1	1	1	1	1	1	1	–	–	–	–	–	–	–	–	–
	Memory devices supported	DDR2, DDR, SDR															

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count and Transceiver Count

E144 pin[4] (22 mm, 0.5 mm pitch)	–	–	–	–	–	–	–	91	91	81	79	–	–	–	–	–
M164 pin (8 mm, 0.5 mm pitch)	–	–	–	–	–	–	–	–	–	89	–	–	–	–	–	–
M256 pin (9 mm, 0.5 mm pitch)	–	–	–	–	–	–	–	–	–	165	–	–	–	–	–	–
U256 pin (14 mm, 0.8 mm pitch)	–	–	–	–	–	–	–	179	179	165	153	–	–	–	–	–
U484 pin (19 mm, 0.8 mm pitch)	–	–	–	–	–	–	–	–	–	–	–	–	328	324	292	–
F169 pin (14 mm, 1.0 mm pitch)	72 2	72 2	72 2	–	–	–	–	–	–	–	–	–	–	–	–	–
F256 pin (17 mm, 1.0 mm pitch)	–	–	–	–	–	–	–	179	179	165	153	–	–	–	–	–
F324 pin (19 mm, 1.0 mm pitch)	–	150 4	150 4	–	–	–	–	–	–	–	–	193	193	–	–	–
F484 pin (23 mm, 1.0 mm pitch)			290 4	290 4	290 4	270 4	270 4	–	–	343	–	328	328	324	292	280
F672 pin (27 mm, 1.0 mm pitch)	–	–	–	310 8	310 8	393 8	393 8	–	–	–	–	–	–	–	–	–
F780 pin (29 mm, 1.0 mm pitch)	–	–	–	–	–	–	–	–	–	–	–	532	532	374	426	528
F896 pin (31 mm, 1.0 mm pitch)	–	–	–	–	–	475 8	475 8	–	–	–	–	–	–	–	–	–

Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. Transceiver performance varies by product line and package offering.
3. EP4CGX30 supports 3.125 Gbps transceivers only in F484 package option.
4. Enhanced thin quad flat pack (EQFP).

72 2 Values on top indicate available user I/O pins; values at the bottom indicate the 2.5 Gbps or 3.125 Gbps transceiver count.

Pin migration (same Vcc, GND, ISP, and input pins). User I/Os may be less than labeled for pin migration.

MAX CPLD Series

MAX V CPLD Features

View device ordering codes on page 62.

	Product Line	MAX V CPLDs[1]						
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
Resources	LEs	40	80	160	240	570	1,270	2,210
	Equivalent macrocells[2]	32	64	128	192	440	980	1,700
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
	User flash memory (Kb)	8	8	8	8	8	8	8
	Logic convertible to memory[3]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Clocks, Maximum I/O Pins, and Architectural Features	Internal oscillator	✓	✓	✓	✓	✓	✓	✓
	Fast power-on reset	✓	✓	✓	✓	✓	✓	✓
	Boundary-scan JTAG	✓	✓	✓	✓	✓	✓	✓
	JTAG ISP	✓	✓	✓	✓	✓	✓	✓
	Fast input registers	✓	✓	✓	✓	✓	✓	✓
	Programmable register power-up	✓	✓	✓	✓	✓	✓	✓
	JTAG translator	✓	✓	✓	✓	✓	✓	✓
	Real-time ISP	✓	✓	✓	✓	✓	✓	✓
	MultiVolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0[4]	
	I/O power banks	2	2	2	2	2	4	4
	Maximum output enables	54	79	79	114	159	271	271
	LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓
	LVDS outputs	✓	✓	✓	✓	✓	✓	✓
	32 bit, 66 MHz PCI compliant	–	–	–	–	–	✓[4]	✓[4]
	Schmitt triggers	✓	✓	✓	✓	✓	✓	✓
	Programmable slew rate	✓	✓	✓	✓	✓	✓	✓
	Programmable pull-up resistors	✓	✓	✓	✓	✓	✓	✓
	Programmable GND pins	✓	✓	✓	✓	✓	✓	✓
	Open-drain outputs	✓	✓	✓	✓	✓	✓	✓
	Bus hold	✓	✓	✓	✓	✓	✓	✓
Package Options and I/O Pins[5]								
E64 pin (9 mm, 0.4 mm pitch)		54	54	54	–	–	–	–
T100 pin[6] (16 mm, 0.5 mm pitch)		–	79	79	79	74	–	–
T144 pin[6] (22 mm, 0.5 mm pitch)		–	–	–	114	114	114	–
M64 pin (4.5 mm, 0.5 mm pitch)		30	30	–	–	–	–	–
M68 pin (5 mm, 0.5 mm pitch)		–	52	52	52	–	–	–
M100 pin (6 mm, 0.5 mm pitch)		–	–	79	79	74	–	–
M144 pin (7 mm, 0.5 mm pitch)		–	–	–	–	–	–	–
M256 pin (11 mm, 0.5 mm pitch)		–	–	–	–	–	–	–
U256 pin (14 mm, 0.8 mm pitch)		–	–	–	–	–	–	–
F100 pin (11 mm, 1.0 mm pitch)		–	–	–	–	–	–	–
F256 pin (17 mm, 1.0 mm pitch)		–	–	–	–	159	211	203
F324 pin (19 mm, 1.0 mm pitch)		–	–	–	–	–	271	271

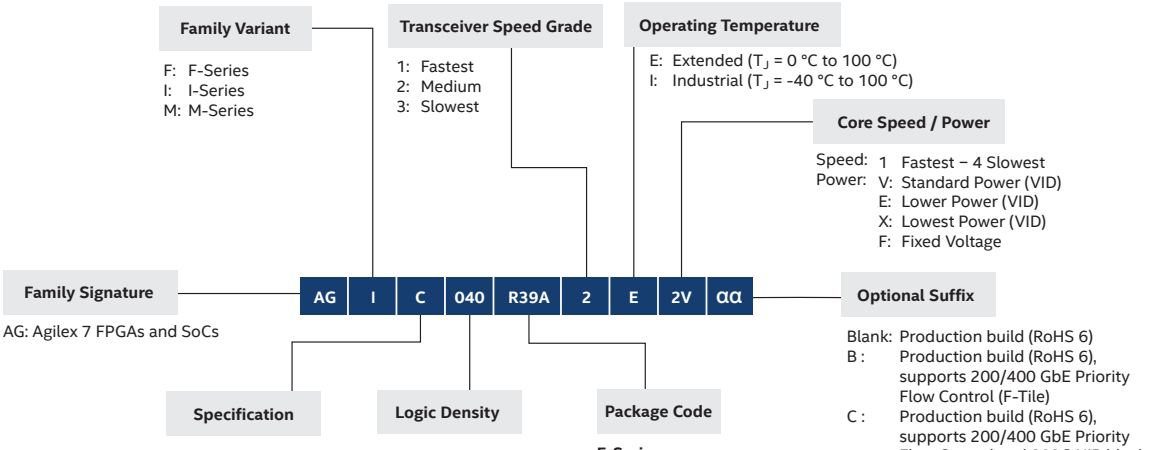
Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. Typical equivalent macrocells.
3. Unused LEs can be converted to memory. The total number of available LE RAM bits depends on the memory mode, depth, and width configurations of the instantiated memory.
4. An external resistor must be used for 5.0 V tolerance.
5. For temperature grades of specific packages (commercial, industrial, or extended temperatures), refer to Intel's online selector guide.
6. Thin quad flat pack (TQFP).

54 Number indicates available user I/O pins.

Pin migration (same Vcc, GND, ISP, and input pins). User I/Os may be less than labeled for pin migration.

Ordering Codes

Ordering Information for Intel Agilex 7 FPGAs F-Series, I-Series and M-Series



Code	HPS	Crypto	HBM2E	Series
A	N	N	None	F, I, M
B	Y	N	None	F, I, M
C[1]	N	Y	None	F, I
D[1]	Y	Y	None	F, I
E	Y	N	16 GB	M
F	Y	N	32 GB	M
G	N	N	16 GB	M
H	N	N	32 GB	M

006: 573K logic elements
008: 764K logic elements
012: 1,178K logic elements
014: 1,437K logic elements
019: 1,918K logic elements
022: 2,208K logic elements
023: 2,308K logic elements
027: 2,692K logic elements
032: 3,245K logic elements
035: 3,540K logic elements
039: 3,851K logic elements
040: 4,047K logic elements
041: 4,000K logic elements

F-Series

R16A = 1546A	F x2
R24B = 2486A	P x1, E x1
R24C = 2340A	F x2
R24D = 2340A	F x1
R25A = 2581A	P x2, E x1
R31C = 3184C	F x4

I-Series

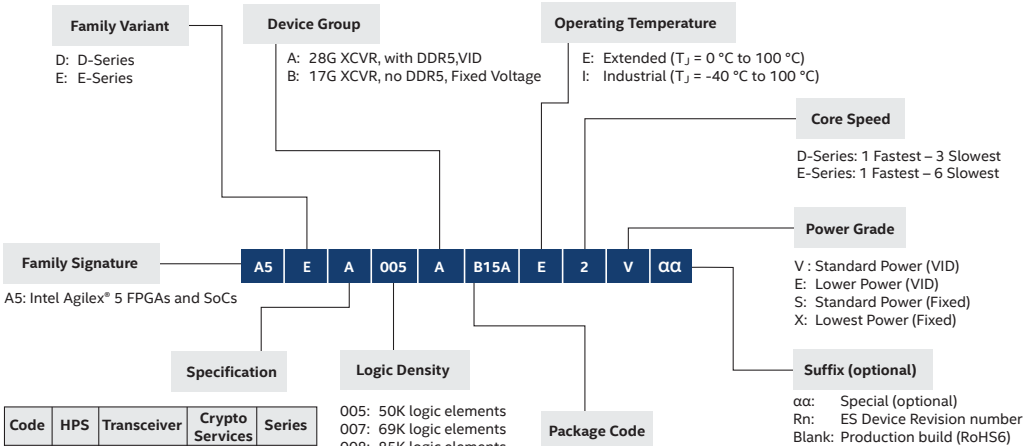
R18A = 1805A	R x1, F x1
R29A = 2957A	R x3, F x1
R29D = 2957A	R x3, F x1
R31A = 3184A	R x1, F x3
R31B = 3184B	F x4
R31E = 3184E	R x2, Fx2
R39A = 3948A	F x6

M-Series

R31B = 3184B	F x4
R47A = 4700A	F x3, R x1, HBM
R47B = 4700B	F x4, HBM

[1] Hard Crypto blocks supported in 019, 023, 035, 040, 041 logic density devices only

Ordering Information for Intel Agilex 5 FPGAs D-Series and E-Series



Code	HPS	Transceiver	Crypto Services	Series
A	N	N	N	E
B	Quad HPS[1]	N	N	E
C	N	Y	N	D, E
D	Quad HPS[1]	Y	N	D, E
E	Dual HPS[2]	N	N	E
G	N	N	Y[3]	E

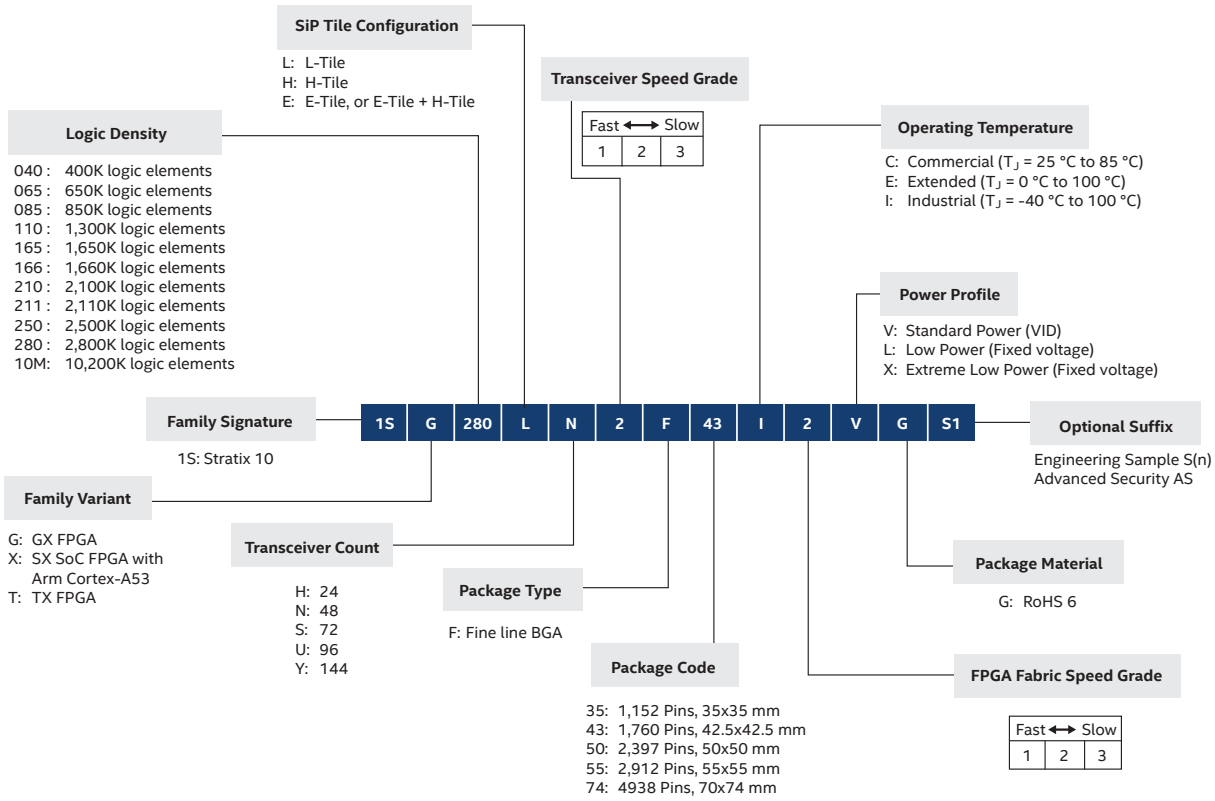
005: 50K logic elements
007: 69K logic elements
008: 85K logic elements
010: 103K logic elements
013: 138K logic elements
025: 252K logic elements
028: 282K logic elements
031: 318K logic elements
043: 434K logic elements
051: 515K logic elements
052: 524K logic elements
064: 644K logic elements
065: 656K logic elements

Package Code	Pins (D-Series)	Pins (E-Series)	Package Size
B15A	NA	324 pins	15 x 15 mm
M16A	NA	896 pins	16 x 16 mm
B18A	NA	474 pins	18 x 18 mm
B23A	820 pins	839 pins	23 x 23 mm
B23B	NA	795 pins	23 x 23 mm
B32A	1,610 pins	1,591 pins	32 x 32 mm

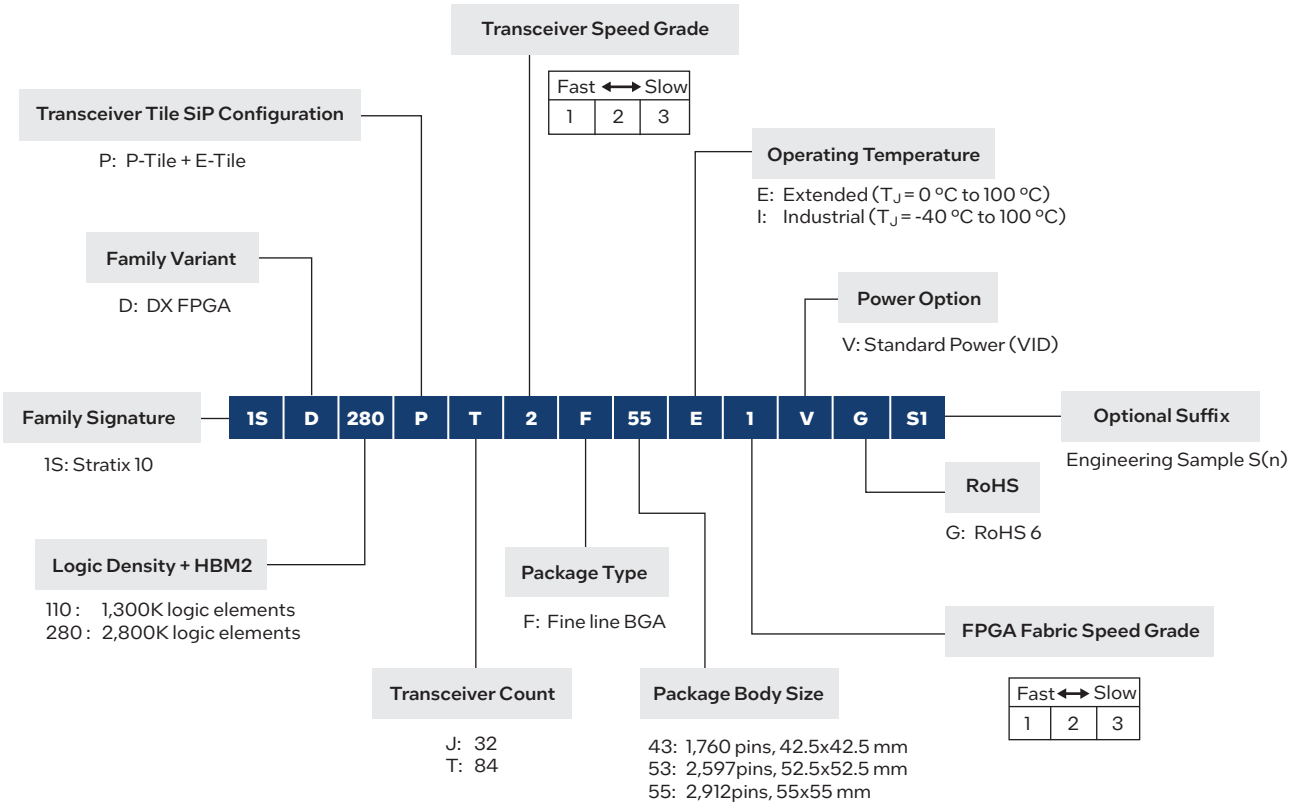
M = 0.5mm Micro Fineline BGA Package
B = Variable Pitch BGA Package

[1] Quad HPS = 2xA55 and 2xA76
[2] Dual HPS = 2XA55
[3] Enabled for B18A pkg only

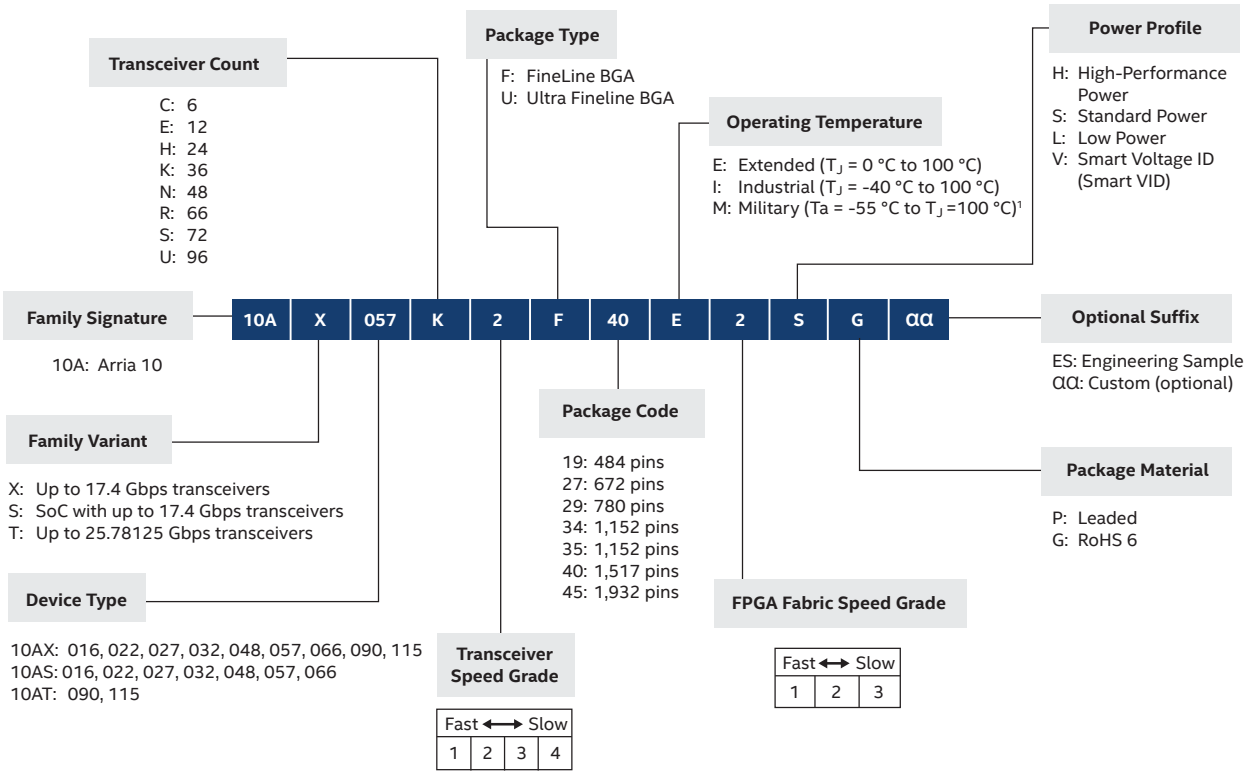
Ordering Information for Intel Stratix 10 (GX, SX, TX) Devices



Ordering Information for Intel Stratix 10 (DX) Devices

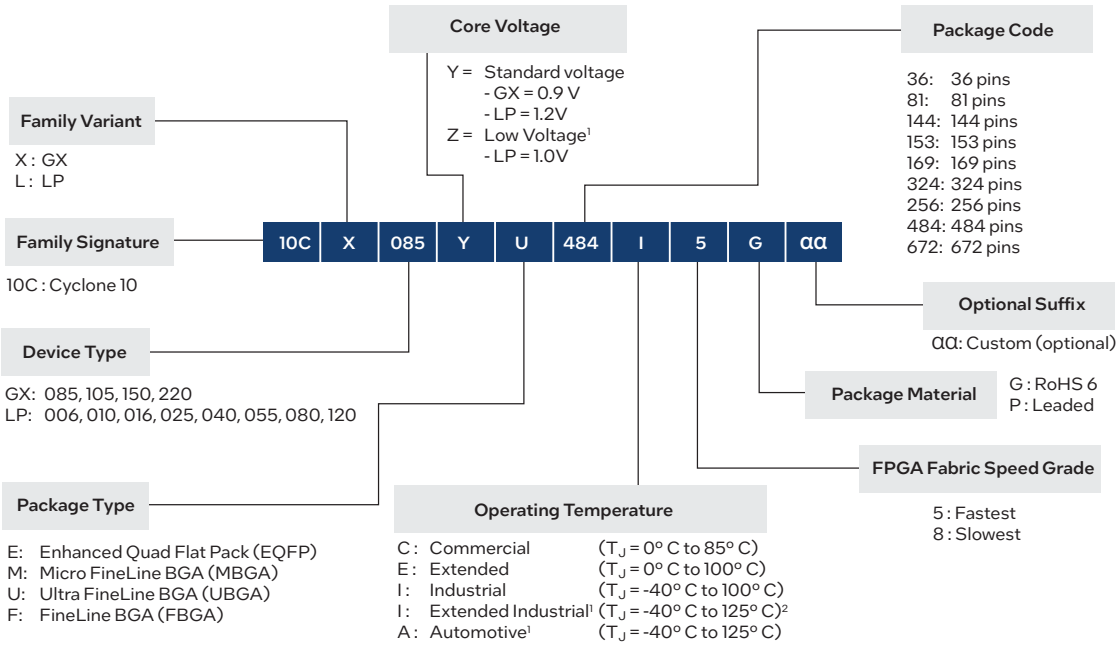


Ordering Information for Intel Arria 10 (GX, SX, GT) Devices



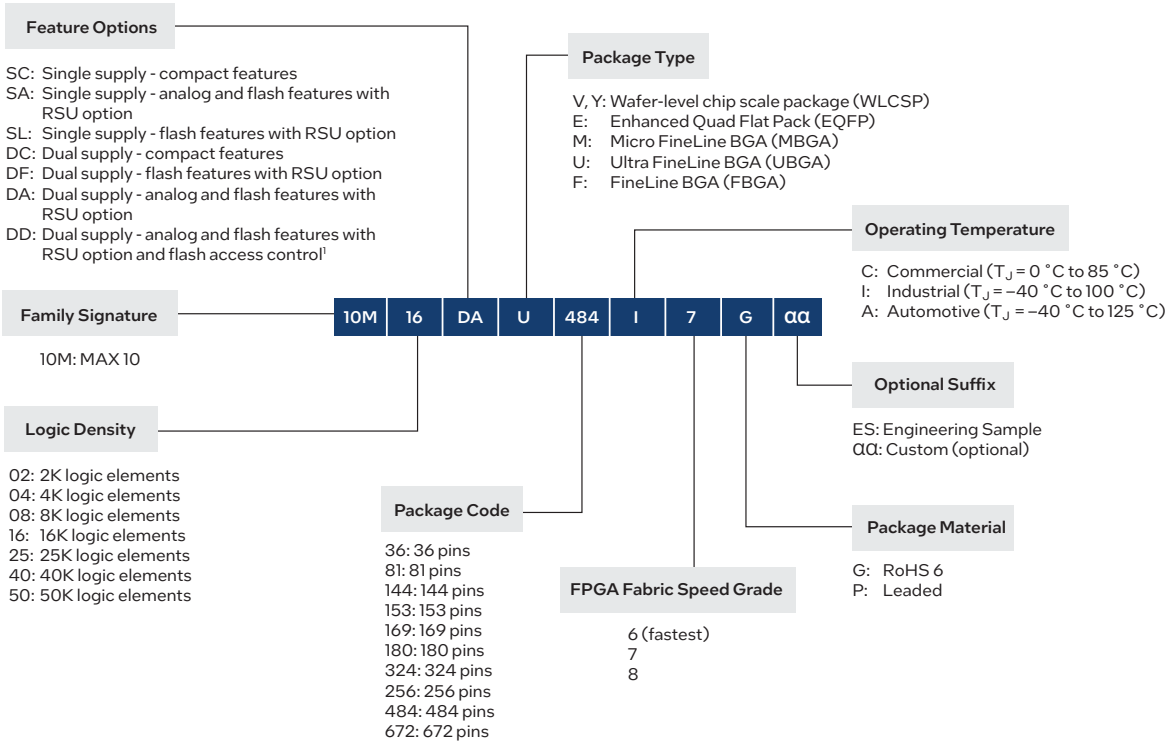
[1] For details, refer to the Intel® Arria® 10 Military Temperature Range Support Technical Brief.

Ordering Information for Cyclone 10 Devices



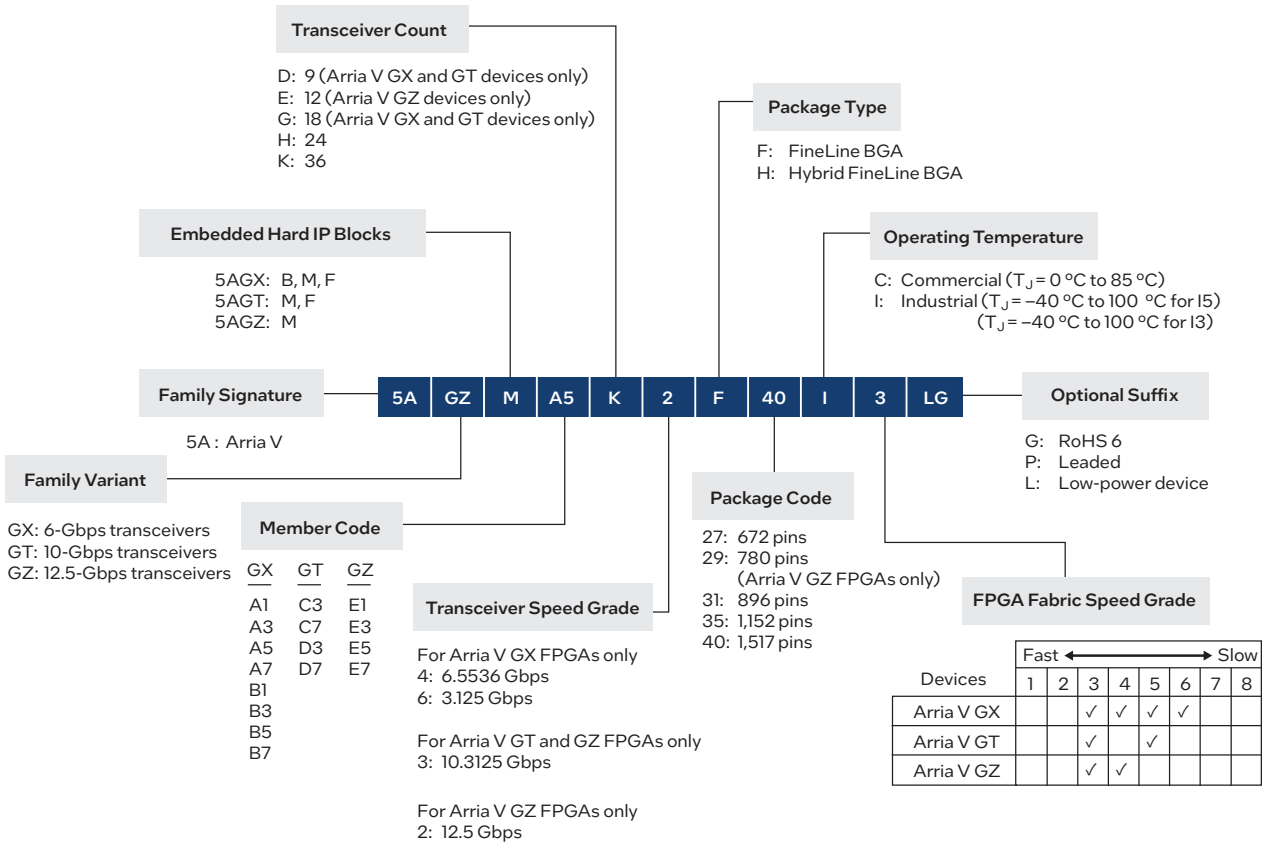
[1] Only available on Intel Cyclone 10 LP.
[2] For details, refer to the Extended Temperature Device Support web page.

Ordering Information for MAX 10 Devices

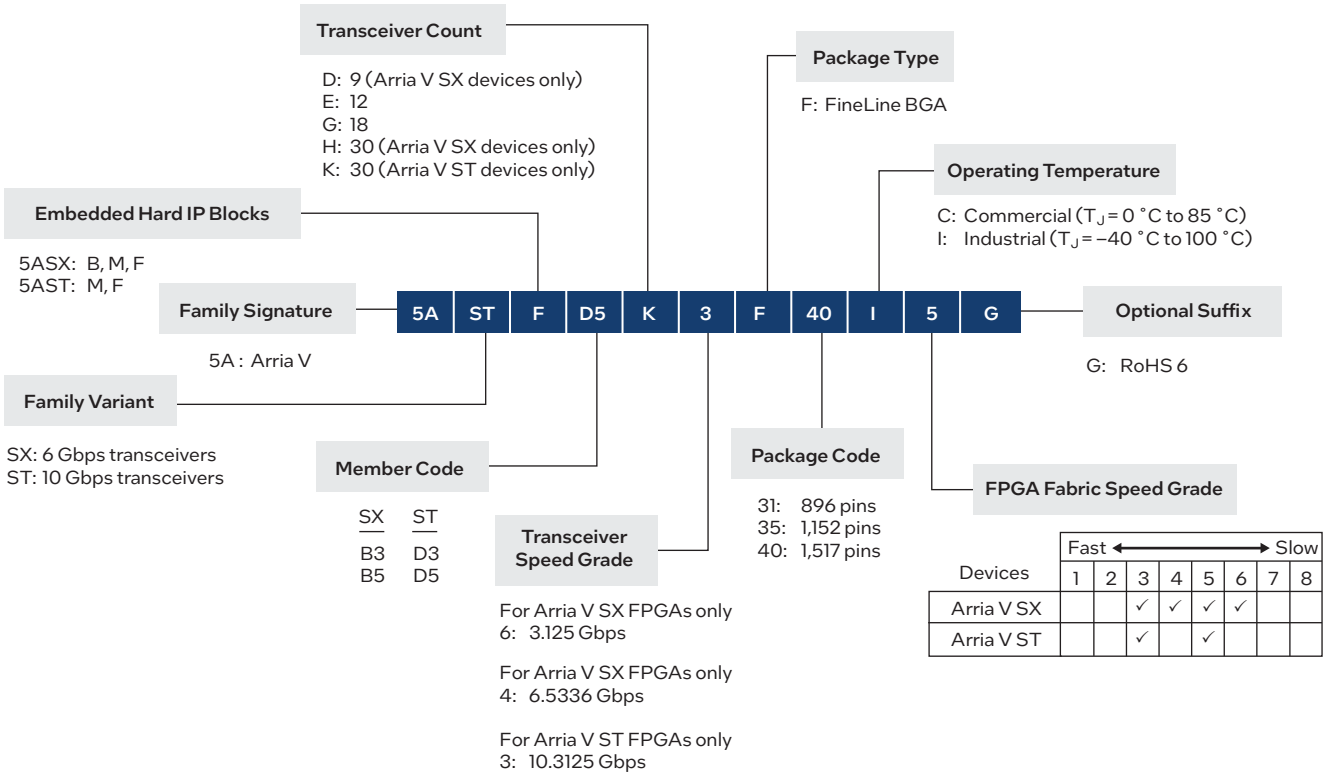


[1] DD OPN available only on 10M40 and 10M50 devices with F256, F484, and F762 packages.

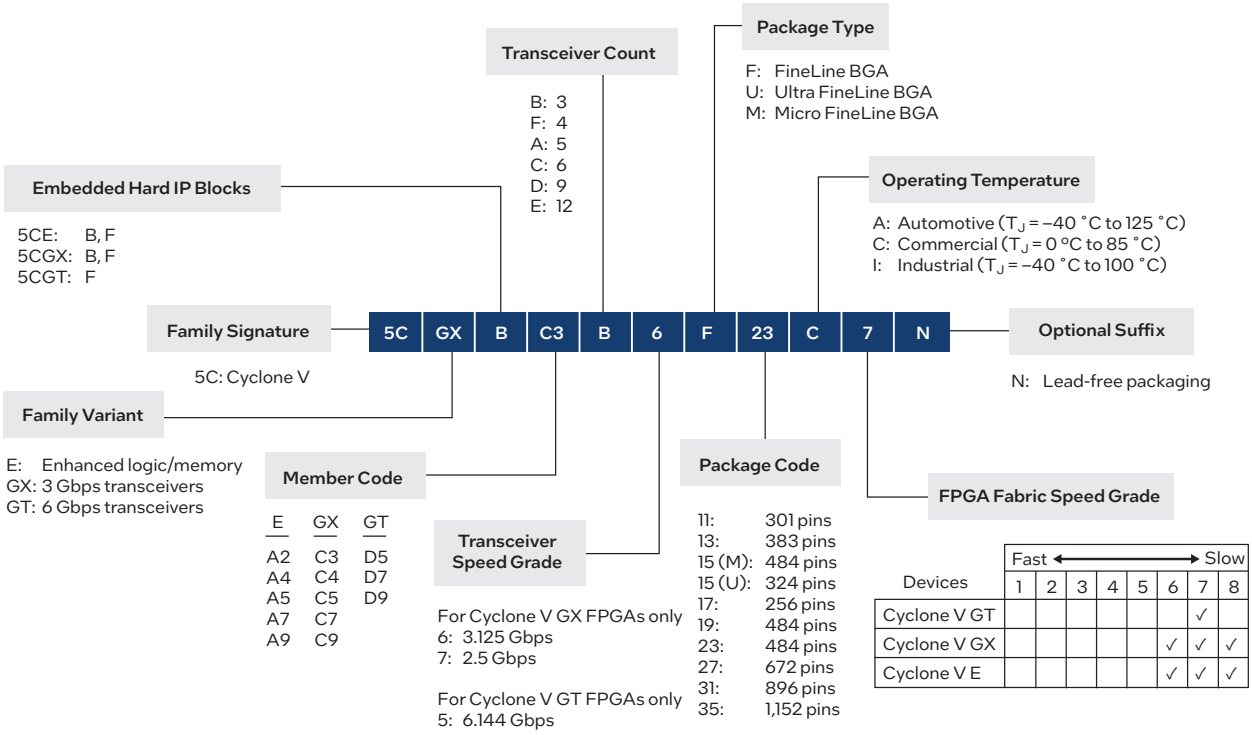
Ordering Information for Arria V (GT, GX, GZ) Devices



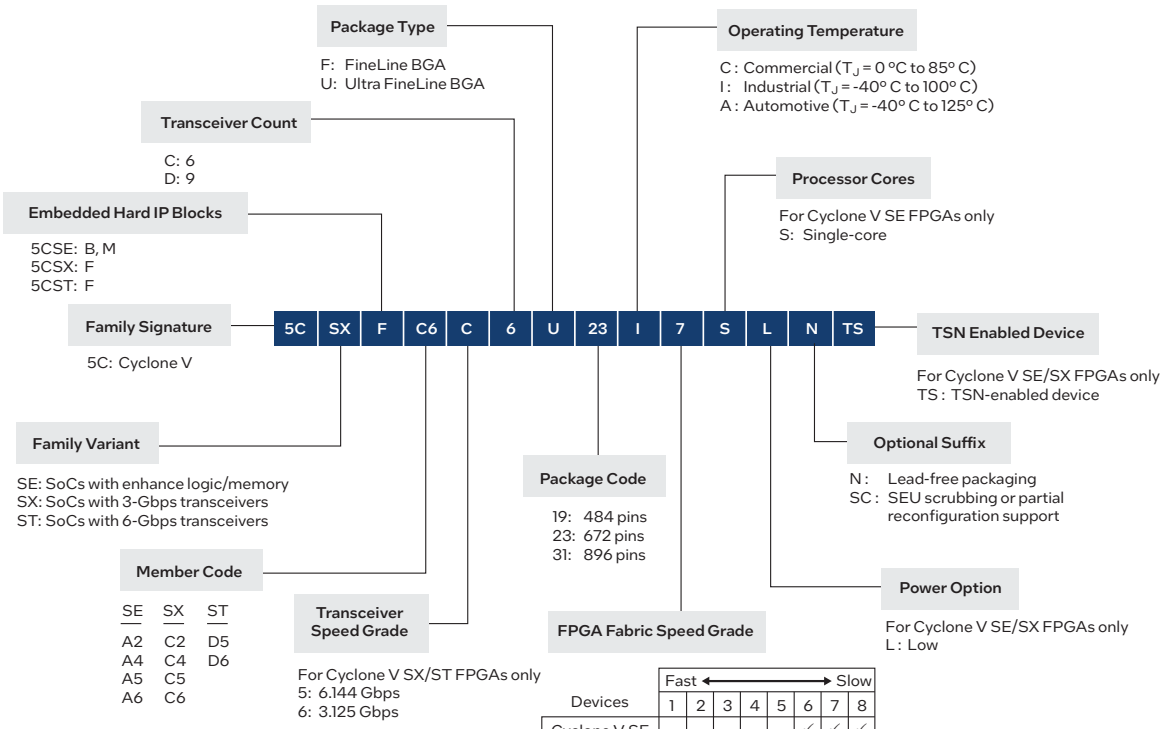
Ordering Information for Arria V (SX, ST) SoCs



Ordering Information for Cyclone V (E, GX, GT) Devices

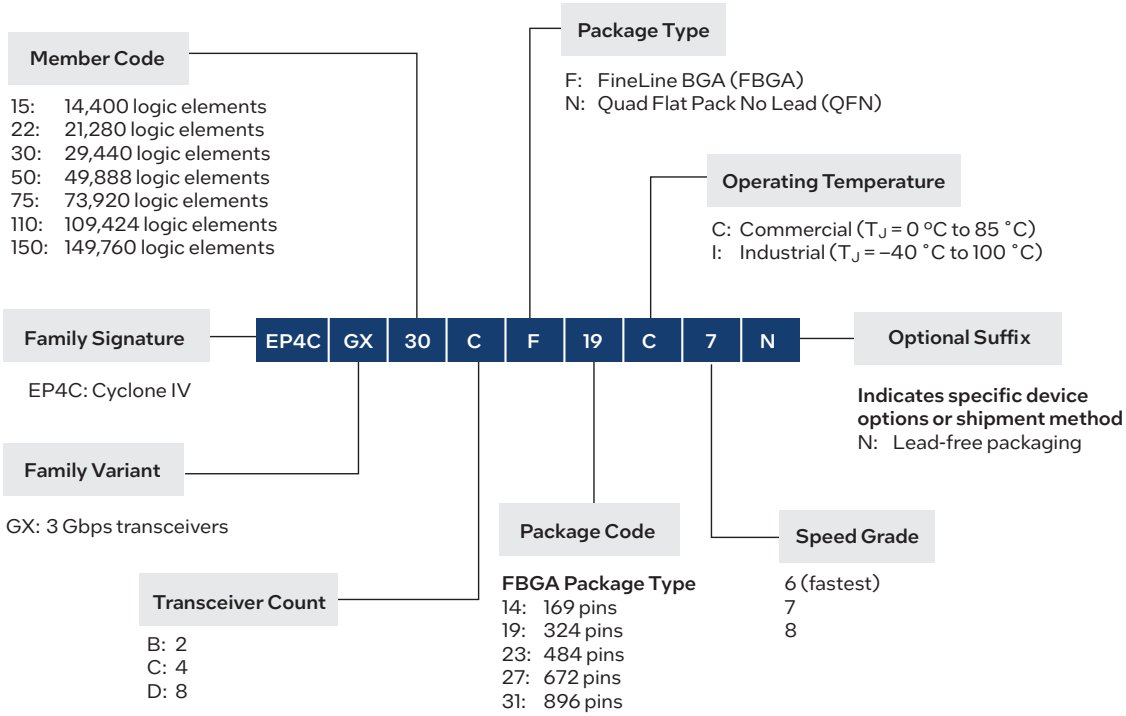


Ordering Information for Cyclone V (SE, SX, ST) SoCs

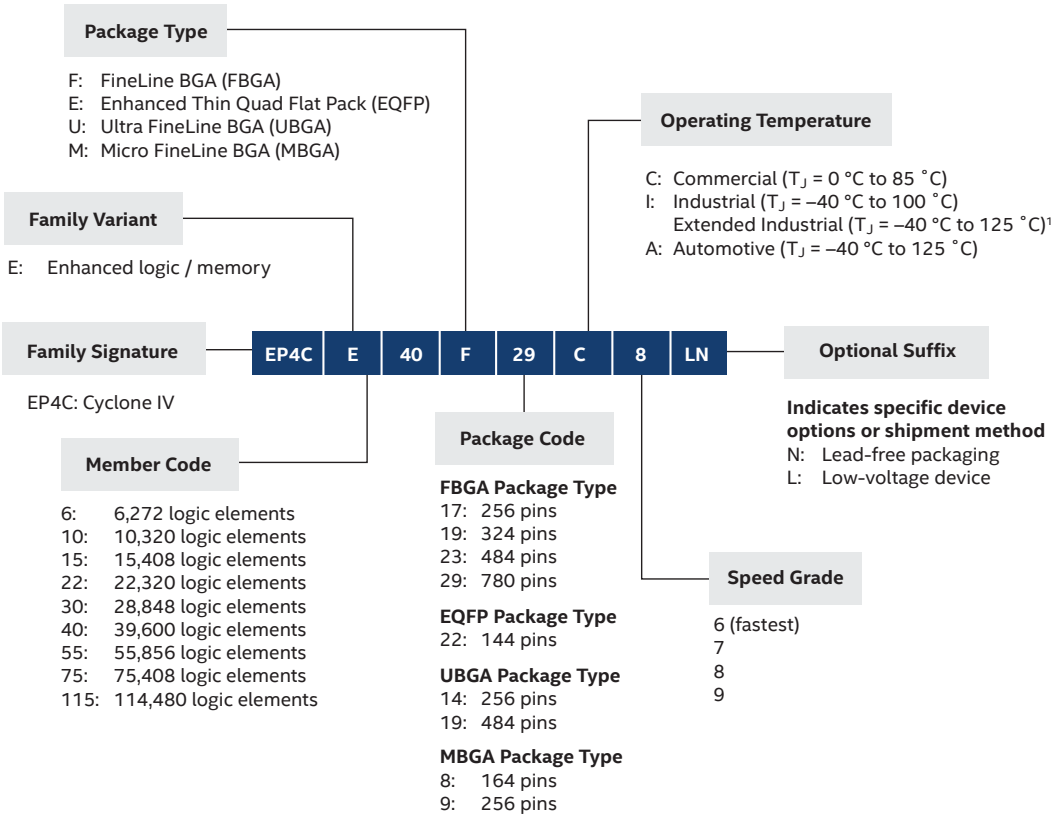


Devices	Fast ← → Slow							
	1	2	3	4	5	6	7	8
Cyclone V SE						✓	✓	✓
Cyclone V SX						✓	✓	✓
Cyclone V ST							✓	

Ordering Information for Cyclone IV GX Devices

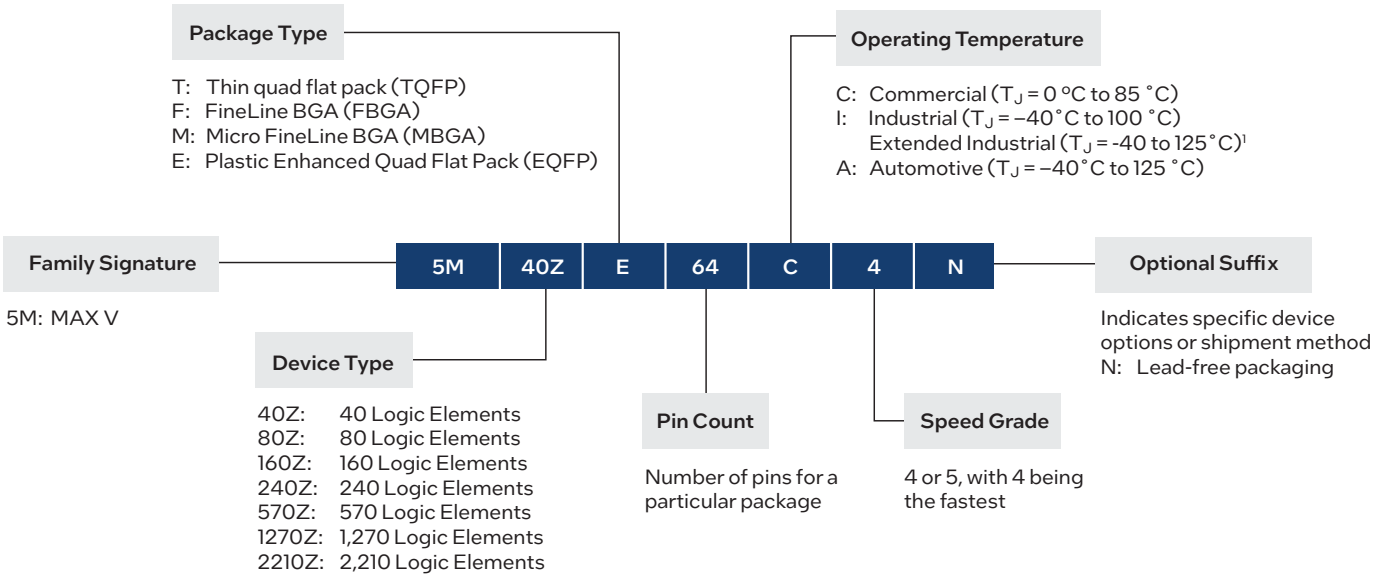


Ordering Information for Cyclone IV E Devices



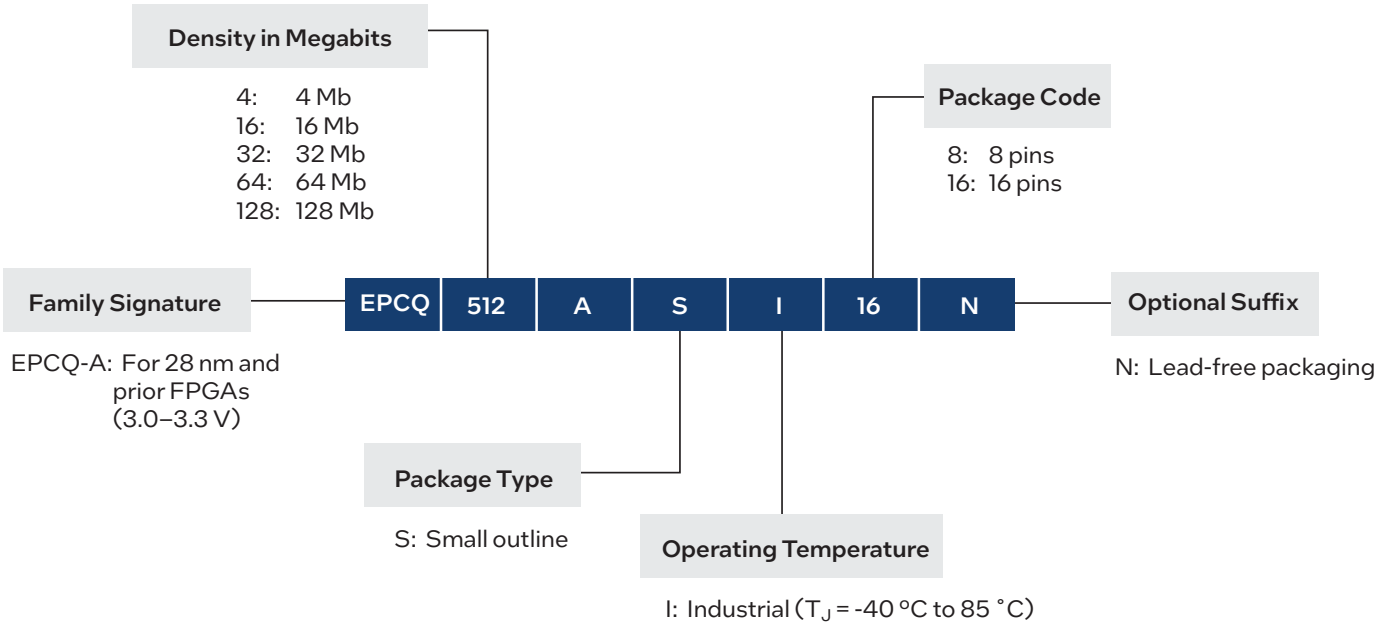
[1] For details, refer to the Extended Temperature Device Support web page.

Ordering Information for MAX V Devices



[1] For details, refer to the Extended Temperature Device Support web page.

Ordering Information for Serial Configuration Devices



Intel FPGA Acceleration Card Solutions

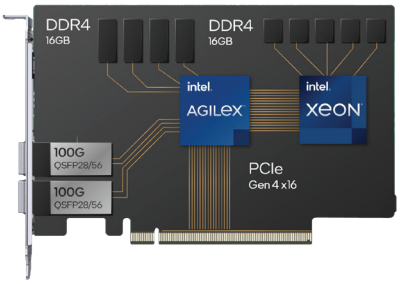
Accelerate your data center, cloud, or network infrastructure with a portfolio of Intel and partner infrastructure processing units (IPUs) and SmartNICs. These acceleration solutions are enabled by Intel's latest FPGA technology, and designed then qualified for large volume deployments. Intel, third-party, and proprietary cards, such as the Intel FPGA IPU F2000X-PL Platform, Intel FPGA SmartNIC N6000-PL Platform, and Silicom FPGA SmartNIC N5010 Series, are supported by next-generation platform software – Open FPGA Stack (OFS). Intel's wide portfolio of platforms, cards, and software solutions enable your workloads to be efficiently developed, scaled, and deployed.

Intel® FPGA SmartNIC and IPU Platforms

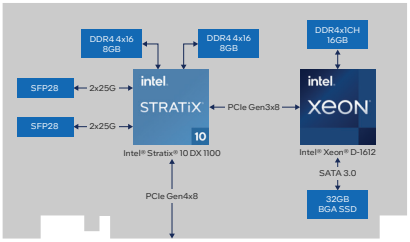
Intel FPGA SmartNIC and IPU platforms are delivered in two ways: as production-ready solutions and as platform designs.

Production-ready solutions can be purchased from Intel partners who offer commercial off-the-shelf production cards and solutions. OFS and baseboard management controller (BMC) design files are available from partners to accelerate workload development.

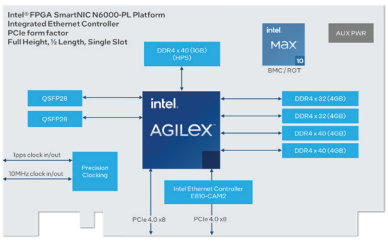
Customers who wish to accelerate their own custom board design can leverage an Intel FPGA SmartNIC or IPU Platform, consisting of board design files, OFS, BMC design files, documentation, and a pre-production board. To get started, contact your local Intel sales representative to learn more.



Intel FPGA IPU F2000X-PL Platform is an Intel Agilex FPGA and Intel Xeon processor-based platform for high-performance cloud acceleration. It offers 2x100 GbE network interfaces and accelerates cloud infrastructure workloads such as Open vSwitch (OvS), Non-Volatile Memory Express over Fabrics (NVME-oF*), and Remote Direct Memory Access (RDMA) over Converged Ethernet v2. Leverage FPGA programmability through OFS with Infrastructure Programmer Development Kit (IPDK), Data Plane Development Kit (DPDK), or Storage Performance Development Kit (SPDK). Production-ready solutions are currently available from Napatech.

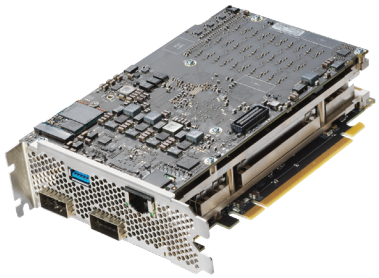


Intel FPGA IPU C5000X-PL Platform is an Intel Stratix 10 FPGA and Intel Xeon processor-based cloud infrastructure acceleration platform with 2x25GbE network interfaces. Production-ready solutions are available through Silicom and Inventec.



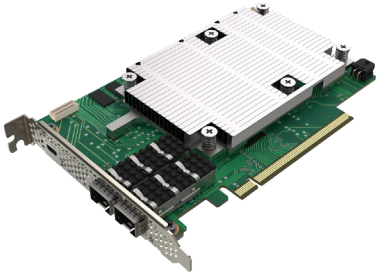
Intel FPGA SmartNIC N6000-PL Platform is Intel's 3rd generation SmartNIC providing 2x100 Gbps Ethernet connectivity and 1588v2 Precision Time Protocol (PTP) synchronization for O-RAN/ Broadcast in a FHHL PCIe form factor. Available workloads include 5G Virtualized Radio Access Network (vRAN), Accelerated Virtual Cell Site Router (vCSR), 5G User Plane Function (UPF), and SMTE ST2110 Offload with JPEG-XS.

Partner FPGA SmartNIC and IPU Production Ready Solutions



Based on the Intel FPGA IPU F2000X-PL Platform

Napatech FPGA IPU F2070X adapter is an IPU based on the Intel Agilex and Intel Xeon D processor, offering both software and hardware programmable data path with 2x100 GbE support and PCIe 4.0 x 16 host interface. With these IPUs, cloud service providers can improve server core utilziation by offloading vSwitch and storage functions using IA-optimzied DPDK and SPDK.



Based on the Intel FPGA IPU C5000X-PL Platform

Silicom FPGA IPU C5010X and Inventec FPGA IPU C5020X adapters are Intel Xeon D processor, SoC + FPGA cards offering a hardware programmable data path with 50G connectivity. With these IPUs, cloud service providers can improve server core utilization by offloading vSwitch and storage using IA-optimized DPDK and SPDK.

Based on the Intel FPGA SmartNIC N6000-PL Platform

Artiza Networks Griffin N6060/N6061, Silicom FPGA SmartNIC N6010/N6011, and WNC FPGA SmartNIC WSN6050 series are high-performance Intel Agilex 7 FPGA F-Series based SmartNICs. These platforms provide 2x100 GbE connectivity and 1588v2 PTP synchronization for acceleration of communication workloads such as 5G vRAN, vCSR, UPF, CN2, and ST2110 Offload.

Silicom FPGA SmartNIC N5010 is the first hardware programmable 4x100 GbE FPGA SmartNIC enabling next-generation IA-based servers to meet the performance needs of the 4/5G Core User Plane Function/Access Gateway Function. Its re-programmability can support Virtual Broadband Network Gateway, Virtualized Evolved Packet Core, Internet Protocol Security, vFirewall, Segment Routing Version, and Vector Packet Processing workload capability.

Product descriptions and datasheets for partner SmartNIC and IPU Acceleration Platforms can be found in the Intel® Solution Marketplace or on the Artiza Networks, Silicom, Inventec, and WNC websites, and are not in this catalog.

Platform Software

OFS is the first complete hardware and software infrastructure that is fully open sourced and comprises composable hardware code and upstreamed kernel code to kernel.org to enable a collaborative community of FPGA developers. OFS provides an efficient approach to customize your own unique acceleration platform solutions using an Intel, 3rd party, or custom board.

All source code and technical documentation is open source in the OFS GitHub and enables development using the Intel Stratix 10 FPGA and Intel Agilex FPGA. To get started, access the OFS GitHub Repositories at www.github.com/OFS or browse our Board Catalog to view all OFS-enabled boards.

Why Choose Intel FPGAs for Acceleration Applications?

Ease of Deployment

Find validated and qualified Intel FPGA SmartNIC and IPU platforms through several leading original equipment manufacturers (OEMs).

Standardization

Help eliminate complexity and enable application portability by leveraging the standard hardware and software interfaces provided by the Intel platform or card software.

Wide-range of Solutions

Discover what FPGAs can do for your business with the broad portfolio of acceleration solutions from technology experts.

Customization

Create customer platform or card solutions using source-accessible OFS hardware and software code.

Faster Time to Deployment

Experience faster time to deployment with native support for OFS by leading open-source software distribution vendors.

Portability

Achieve greater design portability through industry-standard interface support and reusable OFS Standard APIs.

Open FPGA Stack

Open FPGA Stack (OFS) is an open-source hardware and software infrastructure delivered through git repositories that enables you to customize your own unique acceleration platform or workload solutions. OFS provides a starting point and reference infrastructure for custom design by delivering a framework of synthesizable code, a simulation environment, and scripts that can be taken as-is or modified. All OFS source code and technical documentation is open source on GitHub at github.com/OFS. Hardware developers can try out OFS on one of the reference platforms including the Intel Agilex 7 FPGA F-Series Development Kit, Intel Agilex 7 FPGA I-Series Development Kit, Intel FPGA IPU F2000X Platform, or Intel FPGA SmartNIC N6000 Platform before porting to their own boards. Application developers can choose between OFS reference platforms or use the OFS Board Catalog to browse OFS-enabled boards from our ecosystem partners.

OFS provides multiple benefits to hardware, software, and application design engineers:

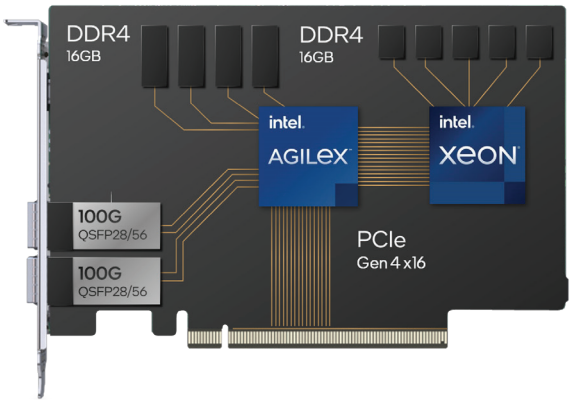
OFS Feature	Board Developer	Software Developer	Application Developer
Inherit an ecosystem of Open FPGA Stack-based boards, workloads, and OS distributors	✓	✓	✓
Accelerate software development by leveraging software drivers upstreamed to the Linux* kernel and Open Programmable Acceleration Engine (OPAE) software and libraries		✓	✓
Accelerate workload development with industry-standard Arm AMBA AXI and Avalon compliant bus interfaces, workload examples, and simulation	✓		✓
Accelerate your verification and validation with automated build scripts, a United Verification Methodology (UVM) environment, and a suite of unit test cases	✓		
Customize your FPGA design (FIM) with modular and composable source code	✓		

Get Started Today with OFS

	Two Routes of Development		
	Using an OFS reference platform	OR	Using a custom or 3rd party board
Step 1: Choose a board	**Intel Agilex FPGA** Intel Agilex 7 FPGA I-Series Development Kit Intel Agilex 7 FPGA F-Series Development Kit Intel IPU F2000X-PL Platform Intel FPGA SmartNIC N6001PL-Platform **Intel Stratix 10 FPGA** D5005 Programmable Acceleration Card		Browse the OFS Board Catalog at www.intel.com/OFS
Step 2: Evaluate OFS open-source resources	Technical documentation can be referenced on GitHub pages www.ofs.github.io		Board vendor will provide a corresponding version of OFS technical documentation
Step 3: Access open-source hardware and software code	Modify or use the provided OFS software or hardware code available at www.github.com/OFS		Board vendor will provide corresponding OFS software or hardware code
Step 4: Develop workload using RTL or C/C++	Follow the OFS RTL flow OR Utilize the oneAPI development flow and build FPGA workloads in C/C++		

Intel FPGA IPU F2000X-PL

The Intel FPGA IPU F2000X-PL is a high-performance Intel Agilex and Intel Xeon D processor based IPU platform providing networking and storage acceleration for cloud and communication service providers. The F2000X-PL offers 2x100GbE network interface and accelerates cloud workloads such as Open vSwitch, NVMe over Fabrics, and RDMA over Converged Ethernet, and has hardware crypto blocks to enhance security. It offers FPGA re-programmability through IPDK, DPDK, SPDK, and OFS.



Targeted Workloads

- Open vSwitch (OvS)
- NVMe-oF
- RDMA over Converged Ethernet v2 (RoCEv2)
- Packet processing
- Cryptographic acceleration
- Security

Hardware

Intel Agilex 7 FPGAs F-Series
- 2,300K logic elements
- 222 Mb on-chip memory
- 3,200 DSP blocks

Intel Xeon D processor
- 8 core Processor
- 15 MB cache
- Up to 3.4 GHz

Onboard memory
- 16 GB DDR4 (to FPGA and processor)

Interfaces
- PCIe 4.0 x16 host interface
- 2X QSFP with up to 2x100 GbE configuration

Form factor
- ¾ length, full height; single slot

Board management
- Intel Cyclone 10 LP FPGA Board Management Controller (BMC)
  - Temperature and voltage readout Platform Level Data Model (PLDM)
- Full security implementation using Intel MAX 10 FPGA as RoT
- Remote update capabilities for FPGA flash memory and BMC

Power management
- Intelligent system power management with real-time telemetry and health monitoring

Software

- IPDK
- DPDK
- SPDK
- OFS[1]

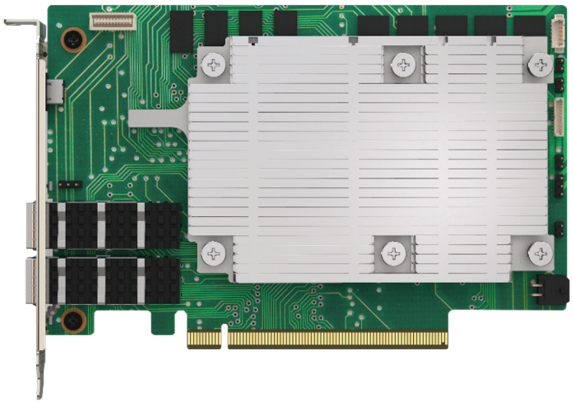
[1] An open-source OFS-based FIM is available. For more information, visit the OFS GitHub.

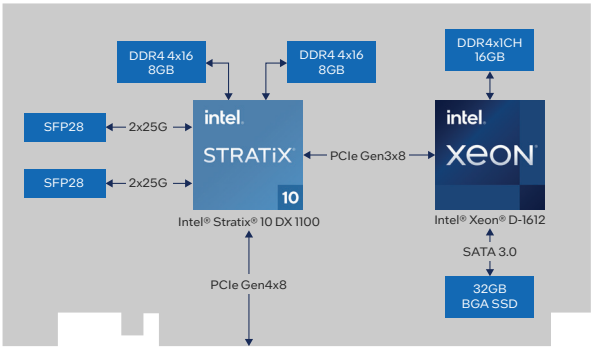
Ordering Information

Contact an Intel sales representative for ordering information.

Intel FPGA IPU C5000X-PL

The Intel FPGA IPU C5000X-PL Platform is a high-performance, Intel Xeon D processor and Intel Stratix 10 FPGA-based, cloud infrastructure accelerator. It supports up to 50G network connectivity and accelerates cloud and telco cloud infrastructure workloads such as Open vSwitch, NVMe over Fabrics, and RDMA over Converged Ethernet v2. Cloud service providers can take advantage of a large software ecosystem including software tools such as Virtio-net and DPDK or SPDK. Workloads can be optimized in bare metal, virtualized cloud, and bare metal virtualization deployments. The development platform is available from Intel, and production ready partner solutions are available from Silicom and Inventec.





Targeted Workloads

- Open vSwitch
- NVMe-oF
- RDMA over Converged Ethernet v2 (RoCEv2)
- Security

Hardware

Intel Stratix 10 DX FPGA
- 1,325K logic elements
- 114 Mb on-chip memory
- 5,184 DSP blocks

Intel Xeon D-1612 processor
- 4 core
- 6 MB cache
- Up to 2.5 GHz

Onboard memory
- 20 GB DDR4
- 1.25 Gb flash

Interfaces
- PCIe 3.0 x8 or 4.0 x8 host interface
- 4-8 core Intel Xeon D processor
- Up to 2x25 GbE configuration

Form factor/thermal/power
- ½ length, full height
- 75 W for key applications

Board management
- Full security implementation using BMC as RoT
- Remote update capabilities for FPGA flash memory and BMC

Power management
- Intelligent system power management with real-time telemetry and system health monitoring

Software

- DPDK/BBDev
- SPDK
- OPAE

Design Entry Tools

- Intel Quartus Prime Pro Edition Software

Ordering Information

Buy now from:
- Inventec, Silicom

Intel FPGA SmartNIC N6000-PL Platform

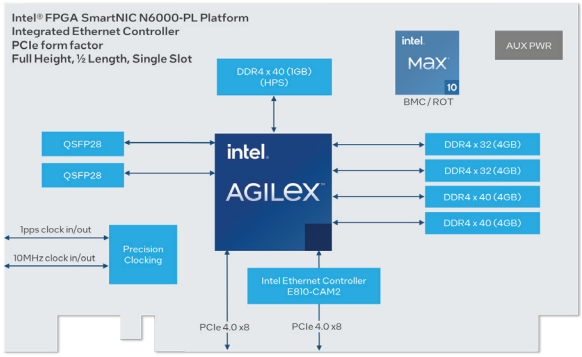
The Intel FPGA SmartNIC N6000-PL Platform is the 3rd generation Agilex 7 FPGA family-based SmartNIC for network acceleration. It supports 2x100 Gbps Ethernet connectivity and 1588v2 PTP synchronization, boasting higher performance, TCO optimization, and scalability compared to previous generations. Intel Agilex 7 FPGAs are built with Intel's advanced 10 nm SuperFin technology and a second-generation Intel Hyperflex FPGA Architecture. Intel Agilex 7 devices deliver ~2X better fabric performance per watt compared to competing 7 nm FPGAs.

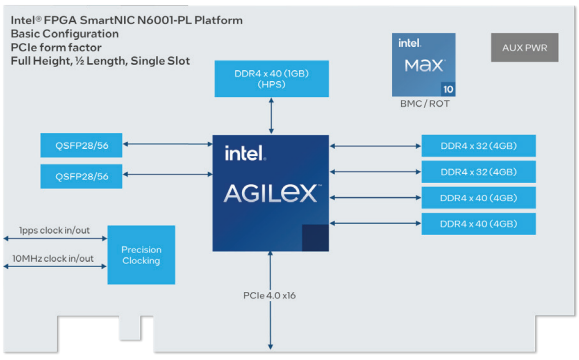
The Intel FPGA SmartNIC N6000-PL Platform is delivered in two ways:

As Production-ready Solutions: Customer who wish to deploy commercial off-the-shelf N6000 based-SmartNIC as-is, can buy N6000-based production cards and solutions from Intel's partners. Open FPGA Stack (OFS) and BMC design files are available from partners to accelerate the workload development

As Platform Design: Customers who wish to accelerate their own custom board design by leveraging the N6000 board design and customizing to add their own differentiation can use the Intel FPGA SmartNIC N6000-PL Platform, consisting of board design files, OFS stack, BMC design files, documentation, and a pre-production board. Contact your local Intel sales representative to learn more.

Workloads Available: 4G/5G Virtualized Radio Access Network (vRAN), Virtual Cell Site Router (vCSR), 5G User Plane Function (UPF), SMPTE ST2110 Professional Media over Managed IP Networks, and more. Contact Intel sales representative or Intel's partners for the workloads.





Targeted Workloads

- vRAN/Open RAN (O-RAN)
- 5G UPF
- vCSR
- SMPTE ST2110 Professional Media over Managed IP Networks

Hardware

Intel Agilex 7 FPGAs F-Series

- High-performance F-Series, multi-gigabit SERDES transceivers up to 58 Gbps
- 1,437K logic elements
- 190 Mb on-chip memory
- 4,510 DSP blocks

Onboard memory

- 16 GB DDR4 to FPGA
- 1 GB DDR4 to HPS

Interfaces

- PCIe 4.0 bifurcated x8/x8 (N6000)
- PCIe 4.0 x16 (N6001)
- Intel® Ethernet Controller E810-CAM2 (N6000)
- 2X QSFP with up to 2x100 GbE support (2x1x100G, 2x2x50G, 2x4x25G, 2x4x10G)
- Supports SyncE, CPRI, eCPRI
- Front panel SMA for IEEE1588 1pps/10 MHz and master clocking
- O-RAN LLS-C1, -C2, -C3 support

Form factor/thermal/power

- FHHL, single slot; passively cooled
- N6000 < 100W, N6001 < 75W
- NEBS Class 1 compliance support

Board management

- Intel MAX 10 FPGA BMC
- Full security implementation using Intel MAX 10 FPGA as RoT
- Remote update capabilities for FPGA flash memory and BMC
- Full card BMC solution host communication via SMBus and PCIe VDM

Power management

- Intelligent system power management with real-time telemetry and system health monitoring

Timing Synchronization

- IEEE 1588v2 support for PRTC/T-GM, T-BC, T-TSC, T-TC
- O-RAN S-Plane PTP support (G.8275.1) for LLS-C1, -C2, -C3, -C4
- Support for Synchronous Ethernet (SyncE)
- Class B frequency and phase timing accuracy
- Integrated OCXO for holdover performance
- Timing interface for local PRTC support for ToD with 1 PPS/10MHz SMA connectors

Software

- DPDK
- FlexRAN/BBDEV(pf-bb-config) - only for vRAN
- OPAE
- OFS

Design Entry Tools

- Intel Quartus Prime Pro Edition Software

Ordering Information

Production card (ready-to-deploy COTS board): Available now

Buy now from:

- Artiza Networks
- Silicom
- Winston NeWeb Corp (WNC)

For Intel FPGA SmartNIC N6000-PL Platform Design (customizing board design)

- Contact Intel sales representative

Accelerated Workload Solutions

Intel's broad ecosystem enables leading providers to offer a variety of accelerator functions best suited for FPGA acceleration. A number of these providers have complete solutions enabled for Intel FPGA-based PACs, IPUs, and SmartNICs, ranging from NFV, network security and monitoring, data analytics, AI, and more.

Networking and Wireless Application Workloads

Virtualized Data Plane Acceleration

Virtualized Radio Access Network (vRAN)

Virtual Cell-site Router (vCSR)

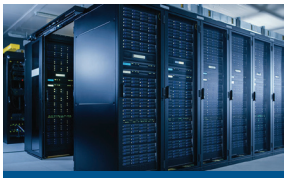
5G User Plane Function (5G UPF)

Enterprise and Cloud Application Workloads

Data Analytics

Artificial Intelligence

Packet Monitoring and Cyber Security



Storage

Media Processing

Financial Services (FSI)

Genomics

Browse Intel® Solutions Marketplace

Or visit the following website for various partner acceleration solutions:
www.intel.com/content/www/us/en/products/details/fpga/platforms.html

Intel FPGA Acceleration Card Comparison

Features		Silicom FPGA SmartNIC N5010	Intel IPU C5000X-PL Platform	Intel FPGA SmartNIC N6000-PL Platform	Intel FPGA IPU F2000X-PL Platform
Product Category	Target Market	SmartNIC for Communications	IPU for CSP	SmartNIC for Communications	IPU for CSP
	Type	Partner card	Partner card	Intel SmartNIC Platform	Intel FPGA IPU
FPGA Resources	FPGA	Intel Stratix 10 DX	Intel Stratix 10 DX	Intel Agilex 7 FPGA F-Series	Intel Agilex 7 FPGA F-Series
	Logic Elements	2,073K	1,325K	1,437K	2,300K
	On-chip Memory	240 Mb	114 Mb	190 Mb	222 Mb
	DSP Blocks	7,920	5,184	4,510	3,200
Processor	Type	-	Intel Xeon D-1612 Processor	Quad-core 64-bit Arm Cortex-A53 Processor	8-core Intel Xeon-D SoC
Memory	DDR4	32 GB	20 GB	16 GB FPGA, 1 GB Processor	16 GB FPGA, 16 GB SoC
	SRAM	144 Mb QDR IV	-	-	-
	Flash	2 Gb	1.25 Gb	-	2 Gb
Interfaces and Modules	PCI Express	4.0 x16 edge connector 4.0 x16 over cable (N5000)	3.0 x8, 4.0 x8 (Option)	4.0 x8 FPGA & 4.0 x8 to E810 Ethernet controller (N6000) 4.0 x16 to FPGA (N6001)	4.0 x16
	Network Interface	4 x100 Gbps Dual Intel Ethernet Controller E810 (N5000)	2 x25 Gbps	2 x 100 Gbps	2x 100 Gbps
	Intel MAX 10 FPGA Board Management Controller	Yes	Option	Yes	F2000 has an option for Intel MAX 10 BMC
	FPGA Interface Manager	Yes	-	Yes	Yes
Mechanical, Thermal, and Power	Form Factor	Full Height, ⅔Length Full height, full length (N5000)	Full Height, ½ Length	Full Height, ½ Length	Full Height, ¾ Length Single slot Optional: Full Height, ½ Length Dual slot
	Width	Single slot (active cooling)	Single slot	Single slot	Single slot
	Maximum Power Consumption (TDP)	194 W	36 W (FPGA) + 22/30 W (Intel Xeon D processor 4C/8C)	100 W (N6000), 75 W (N6001)	150 W
Tools Support	Open FPGA Stack (OFS)	Yes	No	Yes	Yes
	Intel Quartus Prime Software	Yes	Yes	Yes	Yes
	Data Plane Developer Kit (DPDK)	Yes	Yes	Yes	Yes
	Infrastructure Programmer Development Kit (IPDK)	No	No	No	Yes
	Storage Performance Development Kit (SPDK)	No	Yes	No	Yes
	P4 Programmable	No	No	Yes	Yes
	Intel Distribution of OpenVINO™ Toolkit	No	No	No	No
How to buy	Contact	Silicom	Inventec, Silicom	Artiza Networks, Silicom, Winston NeWeb Corporation (WNC)	Napatech

Intel Quartus Prime Design Software

intel.com/quartus

The Intel Quartus Prime Software is revolutionary in performance and productivity for FPGA, CPLD, and SoC designs, providing a fast path to convert your concept into reality. The Intel Quartus Prime Software also supports many third-party tools for synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

Intel Quartus Prime Design Software			Availability		
			Pro Edition ($)	Standard Edition ($)	Lite Edition (Free)
Device Support	Intel Agilex FPGAs		✓		
	Intel Stratix series	IV, V		✓	
		10	✓		
	Intel Arria series	II			✓[1]
		II, V		✓	
		10	✓	✓	
	Intel Cyclone series	IV, V		✓	✓
		10 LP		✓	✓
		10 GX	✓[2]		
	Intel MAX series			✓	✓
Design Flow	Partial reconfiguration		✓	✓[3]	
	Block-based design		✓		
	Incremental optimization		✓		
Design Entry/Planning	IP Base Suite		✓	✓	Available for purchase
	Intel® HLS Compiler		✓	✓	✓
	Platform Designer (Standard)			✓	✓
	Platform Designer (Pro)		✓		
	Design Partition Planner		✓	✓	
	Chip Planner		✓	✓	✓
	Interface Planner		✓		
	Logic Lock regions		✓	✓	
	VHDL		✓	✓	✓
	Verilog		✓	✓	✓
	SystemVerilog		✓	✓[4]	✓[4]
	VHDL-2008		✓	✓[4]	
Functional Simulation	Questa*-Intel® FPGA Starter Edition software		✓	✓	✓
	Questa-Intel FPGA Edition software		✓[5]	✓[5]	✓[5]
Compilation (Synthesis & Place and Route)	Fitter (Place and Route)		✓	✓	✓
	Register retiming		✓	✓	
	Fractal synthesis		✓		
	Multiprocessor support		✓	✓	
Timing and Power Verification	Timing Analyzer		✓	✓	✓
	Design Space Explorer II		✓	✓	✓
	Power Analyzer		✓	✓	✓
	Power and Thermal Calculator		✓[6]		
In-System Debug	Signal Tap Logic Analyzer		✓	✓	✓
	Transceiver toolkit		✓	✓	
	Intel Advanced Link Analyzer		✓	✓	
Operating System (OS) Support	Windows/Linux 64 bit support		✓	✓	✓

Notes:
1. The only Arria II FPGA supported is the EP2AGX45 device.
2. The Intel Cyclone 10 GX device support is available for free in the Pro Edition software.
3. Available for Cyclone V and Stratix V devices only and requires a partial reconfiguration license.
4. For language support, refer to the **Verilog and SystemVerilog Synthesis Support** section of the Intel Quartus Prime Standard Edition User Guide.
5. Requires an additional license.
6. Integrated in the Intel Quartus Prime Software and available as a stand-alone tool. Only supports Intel Agilex and Intel Stratix 10 devices.

Additional Development Tools

Tools	Description
Intel HLS Compiler	• No additional license required. • Now available as a separate download. • Supported with the Intel Quartus Prime Pro Edition Software.
DSP Builder for Intel FPGAs	• Additional licenses are required. • DSP Builder for Intel FPGAs (Advanced Blockset only) is supported with the Intel Quartus Prime Pro Edition Software for Intel Agilex 7, Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices.
Nios II Embedded Design Suite	• No additional licenses are required. • Supported with all editions of the Intel Quartus Prime Software. • Includes Nios II software development tools and libraries.
Intel SoC FPGA Embedded Development Suite (SoC EDS)	• Requires additional licenses for Arm* Development Studio for Intel® SoC FPGA (Arm* DS for Intel® SoC FPGA). • The SoC EDS Standard Edition is supported with the Intel Quartus Prime Lite/Standard Edition Software and the SoC EDS Pro Edition is supported with the Intel Quartus Prime Pro Edition Software.

Intel Quartus Prime Design Software Features Summary

Interface Planner	Enables you to quickly create your I/O design using real time legality checks.
Pin planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
Platform Designer	Accelerates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect based on a network-on-a-chip architecture.
Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Intel and from Intel's third-party IP partners.
Synthesis	Provides expanded language support for System Verilog and VHDL 2008.
Scripting support	Supports command-line operation and Tcl scripting.
Incremental optimization	Offers a faster methodology to converge to design sign-off. The traditional fitter stage is divided into finer stages for more control over the design flow.
Partial reconfiguration	Creates a physical region on the FPGA that can be reconfigured to execute different functions. Synthesize, place, route, close timing, and generate configuration bitstreams for the functions implemented in the region.
Block-based design flows	Provides flexibility of reusing timing-closed modules or design blocks across projects and teams.
Intel Hyperflex FPGA Architecture	Provides increased core performance and power efficiency for Intel Stratix 10 devices.
Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Intel Quartus Prime Software settings to find optimal results.
Extensive cross-probing	Provides support for cross-probing between verification tools and design source files.
Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
Chip planner	Reduces verification time while maintaining timing closure by enabling small, post-placement and routing design changes to be implemented in minutes.
Timing Analyzer	Provides native Synopsys Design Constraint (SDC) support and allows you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
Signal Tap logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
Power Analyzer	Enables you to analyze and optimize both dynamic and static power consumption accurately.
Design Assistant	A design rules checking tool that allows you to get to design closure faster by reducing the number of iterations needed and by enabling faster iterations with targeted guidance provided by the tool at various stages of compilation.
Fractal synthesis	Enables the Intel Quartus Prime Software to efficiently pack arithmetic operations in the FPGA's logic resources resulting in significantly improved performance.
EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, visit intel.com/fpgaedapartners.

Getting Started Steps

Step 1: Download the free Intel Quartus Prime Lite Edition Software
intel.com/quartus

Step 2: Get oriented with the Intel Quartus Prime Software interactive tutorial.
After installation, open the interactive tutorial on the welcome screen.

Step 3: Sign up for training
intel.com/fpgatraining

Purchase the Intel Quartus Prime Software and increase your productivity today.

Intel Quartus Prime Software
Intel Quartus Prime Software (Standard and Pro Edition) and Questa*-Intel® FPGA Edition software are bundled together into one single ordering part number effective October 15, 2021.
SW-ONE-QUARTUS Price: $3,645
The purchase can be applied for Fixed or Floating or Renewal licenses. Refer to the following product advisories for more information: • ADV 2127 Single Ordering Part Number for Intel Quartus Prime Software

Questa-Intel FPGA Edition Software	Questa-Intel FPGA Starter Edition Software
SW-QUESTA-PLUS	SW-QUESTA
$1,995	Free
Questa-Intel FPGA Edition software is available for $1,995	Questa-Intel FPGA Starter Edition is available for free, but requires a license that can be generated at the Self-Service Licensing Center. It is 40% the performance of the Questa-Intel FPGA Edition software.
Refer to the following product advisories for more information: • ADV 2122 Replacement of ModelSim*-Intel® FPGA Edition Software	

DSP Builder for Intel FPGAs

intel.com/dspbuilder

The DSP Builder for Intel FPGAs is a DSP development tool that allows push-button HDL generation of DSP algorithms directly from the MathWorks Simulink environment. This tool adds additional libraries alongside existing Simulink libraries with the DSP Builder for Intel FPGAs (Advanced Blockset) and DSP Builder for Intel FPGAs (Standard Blockset). Intel recommends using the DSP Builder for Intel FPGAs (Advanced Blockset) for new designs. The DSP Builder for Intel FPGAs (Standard Blockset) is not recommended for new designs except as a wrapper for the DSP Builder for Intel FPGAs (Advanced Blockset).

DSP Builder for Intel FPGAs Features

The DSP Builder for Intel FPGAs (Advanced Blockset) offers the following features:

- Arithmetic logic unit (ALU) folding to build custom ALU processor architectures from a flat data-rate design
- High-level synthesis optimizations, auto-pipeline insertion and balancing, and targeted hardware mapping
- High-performance fixed- and floating-point DSP with vector processing
- Auto memory mapping
- Single system clock datapath
- Flexible 'white-box' fast Fourier transform (FFT) toolkit with an open hierarchy of libraries and blocks for users to build custom FFTs

Generate resource utilization tables for all designs without the Intel Quartus Prime Software compile.

Automatically generate projects or scripts for the Intel Quartus Prime Software, the Questa*-Intel FPGA software, Timing Analyzer, and Platform Designer.

Features	DSP Builder for Intel FPGAs (Standard Blockset)	DSP Builder for Intel FPGAs (Advanced Blockset)
High-level optimization		✓
Auto pipeline insertion		✓
Floating-point blocks		✓
Resource sharing		✓
IP-level blocks	✓	✓
Low-level blocks	✓	✓
System integration	✓	✓
Hardware co-simulation	✓	✓

Purchase the DSP Builder for Intel FPGAs to meet high-performance DSP design needs today.

Pricing	Operating System
$1,995 Primary $1,995 Renewal Subscription for one year	Windows/ Linux

Getting Started with the DSP Builder for Intel FPGAs

Step 1: Download the Intel Quartus Prime Pro or Standard Edition Software (intel.com/quartus):
- Pro Edition to target the latest Intel Agilex 7, Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices.
- Standard Edition to target Intel Arria 10, Intel Cyclone 10 LP, Intel MAX 10, Stratix V, and Cyclone V devices.

Step 2: Purchase additional DSP Builder for Intel FPGAs and MATLAB software licenses:
- DSP Builder for Intel FPGAs software license
- MATLAB software license

Step 3: Follow the following required order of installation:
a. Intel Quartus Prime Software
b. MathWorks MATLAB software
c. DSP Builder for Intel FPGAs

Step 4: To view the DSP Builder for Intel FPGAs version history and software requirements, visit the DSP Builder for Intel FPGAs Version History and Software Requirements web page.

Step 5 : To learn how to add your DSP Builder for Intel FPGAs license to your MATLAB installation, refer to the Installing and Licensing DSP Builder for Intel FPGAs web page.

Embedded Software and Tools for Intel SoC FPGA

intel.com/soceds

The Intel SoC FPGA Embedded Development Suite (SoC EDS) is a comprehensive tool suite for embedded software development on Intel SoC FPGAs. It comprises development tools, utility programs, and design examples to jump-start firmware and application software development. The SoC EDS is available in Standard and Pro Editions. The Standard Edition includes extensive support for 28 nm SoC FPGA families, whereas the Pro Edition is optimized to support the advanced features in the next-generation SoC FPGA families. In addition, the SoC EDS works in conjunction with the Arm Development Studio for Intel SoC FPGA (Arm DS for Intel SoC FPGA). This toolkit enables embedded developers to code, build, debug, and optimize in a single Eclipse-based IDE. The Arm DS for Intel SoC FPGA licenses are available in two options: a 30-day evaluation license and a paid Arm DS for Intel SoC FPGA license. The Arm DS for Intel SoC FPGA license is included at no cost with Intel SoC FPGA Development Kits.

Intel SoC FPGA Embedded Development Suite

	Key Features	Availability			
		Standard		Pro	
		Evaluation License	Paid License	Evaluation License	Paid License
Supported Device Families	Cyclone V SoC	✓	✓		
	Arria V SoC	✓	✓		
	Intel Arria 10 SoC	✓	✓	✓	✓
	Intel Stratix 10 SoC			✓	✓
	Intel Agilex SoC			✓	✓
Compiler Tools	Linaro Compiler[1]	✓	✓	✓	✓
	Arm Compiler 5 (included in the Arm DS for Intel SoC FPGA)		✓		
	Arm Compiler 6 (included in the Arm DS for Intel SoC FPGA)		✓		✓
Libraries	Hardware Libraries (HWLIBs)	✓	✓	✓	✓
Other Tools	Quartus Prime Programmer	✓	✓	✓	✓
	Signal Tap Logic Analyzer	✓	✓	✓	✓
	Intel FPGA Boot Disk Utility	✓	✓	✓	✓
	Device Tree Generator	✓	✓	✓	✓
Design Examples	Golden Hardware Reference Design (GHRD) for SoC development kits	✓	✓	✓	✓
	Triple-Speed Ethernet (TSE) with Modular Scatter-Gather Direct Memory Access (mSG-DMA)[2]	✓	✓	✓	✓
	PCI Express Root Port with Message Signal Interrupts (MSI)[2]	✓	✓	✓	✓
	Partial Reconfiguration design example[3]			✓	✓
Host OS Support	Windows 7 64 bit	✓	✓	✓	✓
	Windows 10 64 bit	✓	✓	✓	✓
	Red Hat Linux 6 64 bit	32 bit libraries are required	32 bit libraries are required	32 bit libraries are required	32 bit libraries are required
Ubuntu 18		✓	✓	✓	✓

Arm Development Studio for Intel SoC FPGA

Arm DS for Intel SoC FPGA	Linux application debugging over Ethernet	✓	✓	✓	✓
	Debugging over Intel FPGA Download Cable II • Board bring-up • Device driver development • Operating system (OS) porting • Bare-metal programming • Arm CoreSight trace support		✓		✓
	Debugging over DSTREAM • Board bring-up • Device driver development • OS porting • Bare-metal programming • Arm CoreSight trace support		✓		✓
	FPGA-adaptive debugging • Auto peripheral register discovery • Cross-triggering between CPU and FPGA domains • Arm CoreSight trace support • Access to System Trace Module (STM) events		✓		✓
	Streamline Performance Analyzer support	Limited	✓	Limited	✓

Notes:
1. You have to download the Linaro Compiler.
2. These design examples are only available through Rocketboards.org.
3. For Intel Arria 10 SoC only.
4. Individual components of SoC EDS can now be downloaded from GitHub.
5. Intel has migrated to Arm DS for Intel SoC FPGA. Arm DS for Intel SoC FPGA is no longer a part of SoC EDS and is a separate download from intel.com.

SoC FPGA Operating System Support

Intel and our ecosystem partners offer comprehensive operating system support for Intel SoC FPGA development boards that support the Arm Cortex-A9 processor.

Operating System	Company
Abassi	Code Time Technologies
Android	MRA Digital
AUTOSAR MCAL	Intel
Bare-Metal/Hardware Libraries	Intel
Carrier Grade Edition 7 (CGE7)	MontaVista
DEOS	DDC-I
eCosPro	eCosCentric
eT-Kernel	eSOL
FreeRTOS	FreeRTOS.org
INTEGRITY RTOS	Green Hills Software
Linux	Open Source (rocketboards.org)
Nucleus	Mentor Graphics

Operating System	Company
OSE	Enea
PikeOS	Sysgo
QNX Neutrino	QNX
RTEMS	RTEMS.org
RTXC	Quadros System
ThreadX	Express Logic
uC/OS-II, uC/OS-III	Micrium
uC3 (Japanese)	eForce
VxWorks	Wind River
Wind River Linux	Wind River
Windows Embedded Compact 7	Microsoft (Witekio)

More Information

For the latest on OS support for Intel SoCs, visit intel.com/socecosystem

Nios® V Processor

The Nios® V processor is the next-generation soft processor for Intel FPGAs based on the open-source industry standard RISC-V instruction set architecture (ISA). This processor is available in the Intel Quartus Prime Pro Edition Software starting with version 21.3. There are three variants of the NIos V processor IP. The Nios V/c compact microcontroller which is the smallest processor in the Nios V family of processors, NIos V/m microcontroller which is balanced for size and performance and the Nios V/g General-Purpose processor which is the high performance Nios V processor. You can use the Nios V processor together with the Arm processor in Intel SoCs to create effective multi-processor systems.

With the Nios V processor you can:

- Lower overall system cost and complexity by integrating external processors into the FPGA.
- Target the Intel Agilex, Intel Stratix, Intel Arria, Intel Cyclone, or Intel MAX 10 FPGA, or the FPGA portion of the Intel Agilex, Intel Stratix 10, Intel Arria 10, Arria V, or Cyclone V SoC.
- Leverage the community-maintained ecosystem to get your designs to market faster by choosing from the most up-to-date and modern toolchains, debuggers, and real-time operating system (RTOS) for your software development
- Take advantage of the free license for the Nios V processors core to get started today

Hardware development

- Intel Quartus Prime Pro Edition Software
- Platform Designer
- Signal Tap logic analyzer
- System Console for low-level debugging of Platform Designer systems

Software development

- Software development and debug is supported using the RiscFree* IDE for Intel® FPGAs. This integrated development environment (IDE) includes the full toolchain, IDE, compiler, debugger, and trace support.
- You can also use third party tools of your choice from the open-source ecosystem that work with RISC-V processors

Licensing

A license is required for Nios V processors. The Nios V embedded processor license is available at no cost in the Self-Service Licensing Center.

Getting started

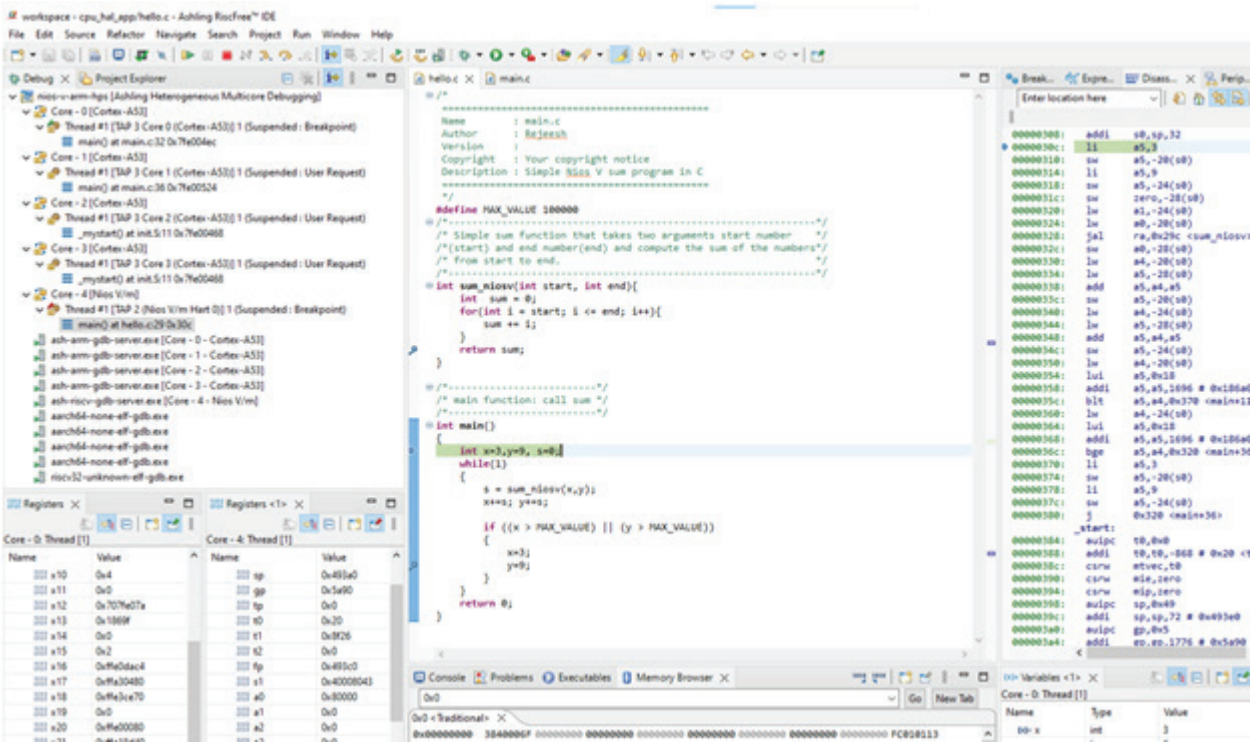
To learn more about the Nios V processor, visit www.intel.com/content/www/us/en/products/details/fpga/nios-processor/v.html

Summary of Soft Processors

Category	Processor	Vendor	Description
Performance and size balanced optimized processing	Nios V microcontroller core	Intel	Nios V processors give you the ultimate flexibility to achieve the exact performance required for your embedded design, without overpaying for high clock frequency, power-hungry off-the-shelf processors. Due to architectural improvements, the Nios V processor has performance benefits over the Nios II processor.
Real-time processing	Nios V General-Purpose Processor	Intel	With unique, real-time hardware features such as custom instructions, ability to use FPGA hardware to accelerate a function, instruction and data caches and tightly coupled memory, as well as support for industry-leading RTOSs, the Nios V processor meets both your hard and soft real-time requirements, and offers a versatile solution for real-time processing.
Size-Optimized processing	Nios V Compact Microcontroller	Intel	Small area footprint for non-interrupt driven area constrained microcontroller applications.

RiscFree* IDE for Intel® FPGAs

The RiscFree* IDE for Intel® FPGAs is developed by Ashling for Intel® FPGAs. This integrated development environment (IDE) provides software development and debug support for Nios V processors that are based on the RISC-V ISA. It includes the full toolchain, IDE, compiler, and debugger.



What you get with RiscFree* IDE with Intel Quartus Prime Software v23.1

- Single-shot free stand-alone installer that works out-of-the-box or integrated with the Intel Quartus Prime Software
- Support for Intel Agilex, Intel Stratix, Intel Arria, Intel Cyclone,or Intel MAX 10 FPGA, or the FPGA portion of the Intel Agilex, Intel Stratix 10, Intel Arria 10, Arria V, or Cyclone V SoC.
- Project Manager and Build Manager including Make and CMake support with rapid import, build, and debug of Intel Quartus software-created applications
- Targeted Nios V GCC compiler toolchain fully integrated into the RiscFree* IDE with support for newlib and picolibc runtime libraries using the Nios V Hardware Abstraction Layer (HAL) application programming interface (API) for hardware access
- Runtime debug with support for the Intel® FPGA Download Cable II
- Homogeneous and heterogeneous simultaneous multi-core debug support for Nios V and Arm processor cores
- Register visualization for Arm processor cores
- uC/OS-II, Zephyr, and FreeRTOS real time operating system debug awareness

Hardware Development Tools

- Intel Quartus Prime Pro Edition Software
- Platform Designer
- Signal Tap logic analyzer
- System Console for low-level debugging of Platform Designer systems

Get Started

The RiscFree* IDE for Intel® FPGAs can be downloaded at FPGA Software Download Center as a stand-alone installer or as part of the Intel Quartus Prime Pro Edition Software download. To learn more about the Nios V processor and the RiscFree* IDE for Intel® FPGAs, visit intel.com/content/www/us/en/products/details/fpga/nios-processor/v.html.

Customizable Processor Portfolio Overview

Performance and Feature Set Summary of Key Processors Supported on Intel FPGAs

Category	Performance-optimized core	Cost sensitive processors	Real-Time Processor	Applications Processors		
Features	Nios V/m Microcontroller	Nios V/c Compact Microcontroller	Nios V/g General Purpose	28 nm[1] Dual-Core Arm Cortex-A9	20 nm[2] Dual-Core Arm Cortex-A9	14 nm[2] Quad-Core Arm Cortex-A53
Maximum frequency (MHz)[3]	~ 566 MHz (Agilex FPGA)[4]	449 (Agilex 7)	334 (Agilex 7)	925 MHz (Cyclone V SoC) 1.05 GHz (Arria V SoC)	1.5 GHz (Intel Arria 10 -1 speed grade)	1.5 GHz (Intel Stratix and Intel Agilex FPGAs)
Agilex 5 (MIPS at MHz)	217 (at 346 MHz)	84 (at 371 MHz)	326 (at 255MHz)	–	–	–
Maximum performance (MIPS at MHz) Intel Agilex device series	268 (at 566 MHz)	102 (at 449 MHz)	426 (at 334 MHz)	–	–	–
Maximum performance (MIPS[5] at MHz) Intel Stratix series	167 (at 360 MHz)	83 (at 368 MHz)	351 (at 275 MHz)	–		–
Maximum performance (MIPS[5] at MHz) Intel Arria series	141 (at 305 MHz)	76 (at 336 MHz)	306 (at 240 MHz)	2,625 MIPS per core at 1.05 GHz	3,750 MIPS per core at 1.5 GHz	–
Maximum performance (MIPS[5] at MHz) Intel Cyclone series	–	68 (at 303 MHz)	301 (at 236 MHz)	2,313 MIPS per core at 925 MHz	–	–
Maximum performance efficiency (MIPS[5] per MHz)	0.63	0.227	1.276	2.5	2.5	2.3
16/32/64 bit instruction set support	32	32	32	16 and 32	16 and 32	16/32/64
Level 1 instruction cache	–	–	Configurable	32 KB	32 KB	32 KB
Level 1 data cache	–	–	Configurable	32 KB	32 KB	32 KB
Level 2 cache	–	–	–	512 KB	512 KB	1 MB
Memory management unit	–	–	–	✓	✓	✓(+System MMU)
Floating-point unit	–	–	Single precision	Dual precision	Dual precision	Dual precision
Vectored interrupt controller	–	–	Future	–	–	–
Tightly coupled memory	–	–	Configurable	–	–	–
Custom instruction interface	–	–	Up to 256	–	–	–
Equivalent ALMs	1,300	427	1,989 - 2,099	HPS	HPS	HPS

Notes:
1. 28 nm SoCs comprise Cyclone V SoCs and Arria V SoCs.
2. 20 nm SoCs comprise Intel Arria 10 SoCs.
3. Maximum performance measurements measured on Stratix V FPGAs.
4. Nios V processor Fmax is based on the highest speed grade device.
5. Dhrystone 2.1 benchmark. Note that performance will vary with system and software configuration.

Intel and Intel Partner Alliance IP Functions

For a complete list of IP functions from Intel and Intel Partner Alliance, please visit intel.com/fpgaip.

	Product Name	Vendor Name
DSP	**Arithmetic**	
	Floating Point Intel FPGA IP	Intel
	Floating Point Arithmetic Co-Processor	Digital Core Design
	Floating Point Arithmetic Unit	Digital Core Design
	Error Detection/Correction	
	POLAR Encoder / Decoder	Intel
	Reed-Solomon Encoder/Decoder II	Intel
	Viterbi Compiler, High-Speed Parallel Decoder	Intel
	Viterbi Compiler, Low-Speed/ Hybrid Serial Decoder	Intel
	Turbo Encoder/Decoder	Intel
	High-Speed Reed Solomon Encoder/ Decoder	Intel
	BCH Encoder/Decoder	Intel
	Low-Density Parity Check Encoder/ Decoder	Intel
	Zip-Accel-C: GZIP/ZLIB/Deflate Data Compression Core	CAST, Inc.
	Zip-Accel-D: GUNZIP/ZLIP/Inflate Data Decompression Core	CAST, Inc.
	Filters and Transforms	
	Fast Fourier Transform (FFT)/ Inverse FFT (IFFT)	Intel
	Cascaded Integrator Comb (CIC) Compiler	Intel
	Finite Impulse Response (FIR) Compiler II	Intel
	SHA-1	CAST, Inc.
	SHA-256	CAST, Inc.
	AES CODECs	CAST, Inc.
	Modulation/Demodulation	
	Numerically Controlled Oscillator Compiler	Intel
	ATSC and Multi-Channel ATSC 8-VSB Modulators	Commsonic
	DVB-T Modulator	Commsonic
	DVB-S2 Modulator	Commsonic
	Video and Image Processing	
	Video and Image Processing Suite	Intel
	Stereo Vision IP Suite	Fujisoft Incorporated
	Infinivision	Gidel
	HD JPEG 2000 Encoders/Decoders	IntoPIX
	TICO Lightweight Video Compression	IntoPIX
	Multi-Channel JPEG 2000 Encoder and Decoder Cores	Silex Insight
	VC-2 High Quality Video Decoder	Silex Insight
	VC-2 High Quality Video Encoder	Silex Insight

	Product Name	Vendor Name
DSP (Continued)	**Video and Image Processing (Continued)**	
	JPEG Encoders	CAST, Inc.
	Ultra-fast, 4K-compatible, AVC/ H.264 Baseline Profile Encoder	CAST, Inc.
	Low-Power AVC / H.264 Baseline Profile Encoder	CAST, Inc.
	H.265 Main Profile Video Decoder	CAST, Inc.
Processors and Peripherals	**Hard/Soft Processors**	
	Nios II Embedded Processors	Intel
	Arm Cortex-A9 MPCore Processor in Intel SoC	Intel
	Arm Cortex-A53 MPCore Processor in Intel SoC	Intel
Interface and Protocols	**Communication**	
	Optical Transport Network (OTN) Framers/Deframers	Intel
	SFI-5.1	Intel
	Ethernet	
	200G MACsec	Intel
	200G Symmetric Cryptographic (AES)	Intel
	Low-Latency 10 Gbps Ethernet Media Access Controller (MAC) with 1588	Intel
	Triple-Speed Ethernet (10/100/1000 Mbps) MAC and PHY with 1588 Option	Intel
	1 / 2.5 / 5 / 10G Multi-Rate PHY and Backplane Options	Intel
	10G Base-X (XAUI) PHY	Intel
	25G MAC and PHY with RS-FEC option	Intel
	40G Ethernet MAC and PHY with 1588 and Backplane Options	Intel
	50G MAC and PHY	Intel
	100G Ethernet MAC and PHY with 1588 and RS-FEC options	Intel
	1G/10Gb Ethernet PHY	Intel
	High-Performance Gigabit Ethernet MAC	IFI
	High Speed	
	eCPRI	Intel
	O-RAN	Intel
	JESD204B	Intel
	JESD204C	Intel
	Common Public Radio Interface (CPRI)	Intel
	Interlaken	Intel
	Interlaken Look-Aside	Intel
	SerialLite II/III/IV	Intel
	SATA 1.0/SATA 2.0	Intelliprop, Inc.
	RapidIO Gen3	Mobiveil
	QDR Infiniband Target Channel Adapter	Polybus

	Product Name	Vendor Name
Interface and Protocols (Continued)	**PCI Express / PCI**	
	PCI Express Hard-IP Controller 3.0, 2.0, 1.0 x1 x2 x4 x8 x16 Controller with SR-IOV on Intel Stratix 10 GX FPGA	Intel
	PCI Express Hard-IP Controller 4.0, 3.0, 2.0, 1.0 x16 x8, x4 x2 x1 Controller with SR-IOV on Intel Stratix 10 DX FPGA	Intel
	PCI Express Hard-IP Controller 5.0, 4.0, 3.0, 2.0, 1.0 x16 x8, x4 x2 x1 Controller with SR-IOV on Intel Agilex FPGA	Intel
	PCI Express Memory-mapped bridge/ DMA IP on Intel Stratix 10 GX, Intel Stratix 10 DX, and Intel Agilex FPGAs	Intel
	PCI Express 4.0, 3.0, 2.0, 1.0 Scalable Switch IP with 1 UP port and up to 32 DN ports for Intel Stratix 10 and Intel Agilex FPGAs	Intel
	Multichannel DMA IP for Intel Stratix 10 GX, Intel Stratix 10 DX, and Intel Agilex FPGAs	Intel
	Expresso 3.0 PCI Express Core (1.0 -4.0)	Rambus (Northwest Logic)
	XpressRICH3 PCI Express 1.0, 2.0, 3.0, and 4.0	PLDA
	CXL	
	XpressLINK-SOC Controller IP for CXL 3.0, 4.0, 5.0 Endpoint & Rootport for Intel Agilex FPGAs	PLDA
	Serial	
	Generic QUAD SPI Controller	Intel
	Avalon® I²C (Master)	Intel
	I²C Slave to Avalon-MM Master Bridge	Intel
	Serial Peripheral Interface (SPI)/Avalon Master Bridge	Intel
	UART	Intel
	JTAG UART	Intel
	16550 UART	Intel
	JTAG/Avalon Master Bridge	Intel
	CAN 2.0/FD	CAST, Inc.
	Local Interconnect Network (LIN) Controller	CAST, Inc.
	H16550S UART	CAST, Inc.
	MD5 Message-Digest	CAST, Inc.
	Smart Card Reader	CAST, Inc.
	DI2CM I²C Bus Interface-Master	Digital Core Design
	DI2CSB I²C Bus Interface-Slave	Digital Core Design
	D16550 UART with 16-Byte FIFO	Digital Core Design
	DSPI Serial Peripheral Interface Master/ Slave	Digital Core Design
	Secure Digital (SD)/MMC SPI	El Camino GmbH
	Secure Digital I/O (SDIO)/SD Memory/ Slave Controller	Eureka Technology, Inc.
	SDIO/SD Memory/ MMC Host Controller	Eureka Technology, Inc.
	Nios II Advanced CAN	IFI
	I²C Master/Slave/PIO Controller	Microtronix, Inc.
	I²C Master and Slave	SLS

	Product Name	Vendor Name
Interface and Protocols (Continued)	**Serial (CONTINUED)**	
	USB High-Speed Function Controller	SLS
	USB Full-/Low-Speed Function Controller	SLS
	Embedded USB 3.0 / 3.1 Gen 1 Host and Device Controllers	SLS
	USB 3.0 SuperSpeed Device Controller	SLS
	Audio and Video	
	Character LCD	Intel
	Pixel Converter (BGR0 to BGR)	Intel
	Video Sync Generator	Intel
	SD/HD/3G-HD Serial Digital Interface (SDI)	Intel
	DisplayPort 1.1 and 1.2	Intel
	HDMI 1.4 and 2.0	Intel
	Bitec HDMI 2.0a IP core	Bitec
	DisplayPort 1.3 IP Core	Bitec
	HDCP IP Core	Bitec
	MIPI CSI-2 Controller Core	Rambus (Northwest Logic)
	MIPI DSI-2 Controller Core	Rambus (Northwest Logic)
	AC'97 Controller	SLS
Memories and Memory Controllers	**DMA**	
	DMA Controllers	Eureka Technology, Inc.
	Lancero Scatter-Gather DMA Engine for PCI Express	Microtronix, Inc.
	AXI DMA back-End Core	Rambus (Northwest Logic)
	Expresso DMA Bridge Core	Rambus (Northwest Logic)
	Express DMA Core	Rambus (Northwest Logic)
	Flash	
	CompactFlash (True IDE)	Intel
	EPCS Serial Flash Controller	Intel
	Flash Memory	Intel
	NAND Flash Controller	Eureka Technology, Inc.
	Universal NVM Express Controller (UNEX)	Mobiveil, Inc.
	ONFI Controller	SLS
	Enhanced ClearNAND Controller	SLS
	SDRAM	
	DDR/DDR2 and DDR3/DDR4 SDRAM Controllers	Intel
	LPDDR2 SDRAM Controller	Intel
	RLDRAM 2 Controller	Intel
	Streaming Multi-Port SDRAM Memory Controller	Microtronix, Inc.
	HyperDrive Multi-Port DDR2 Memory Controller	Microtronix, Inc.
	Avalon Multi-Port SDRAM Memory Controller	Microtronix, Inc.
	SRAM	
	SSRAM (Cypress CY7C1380C)	Intel
	QDR II/II+/II+Xtreme/IV SRAM Controller	Intel

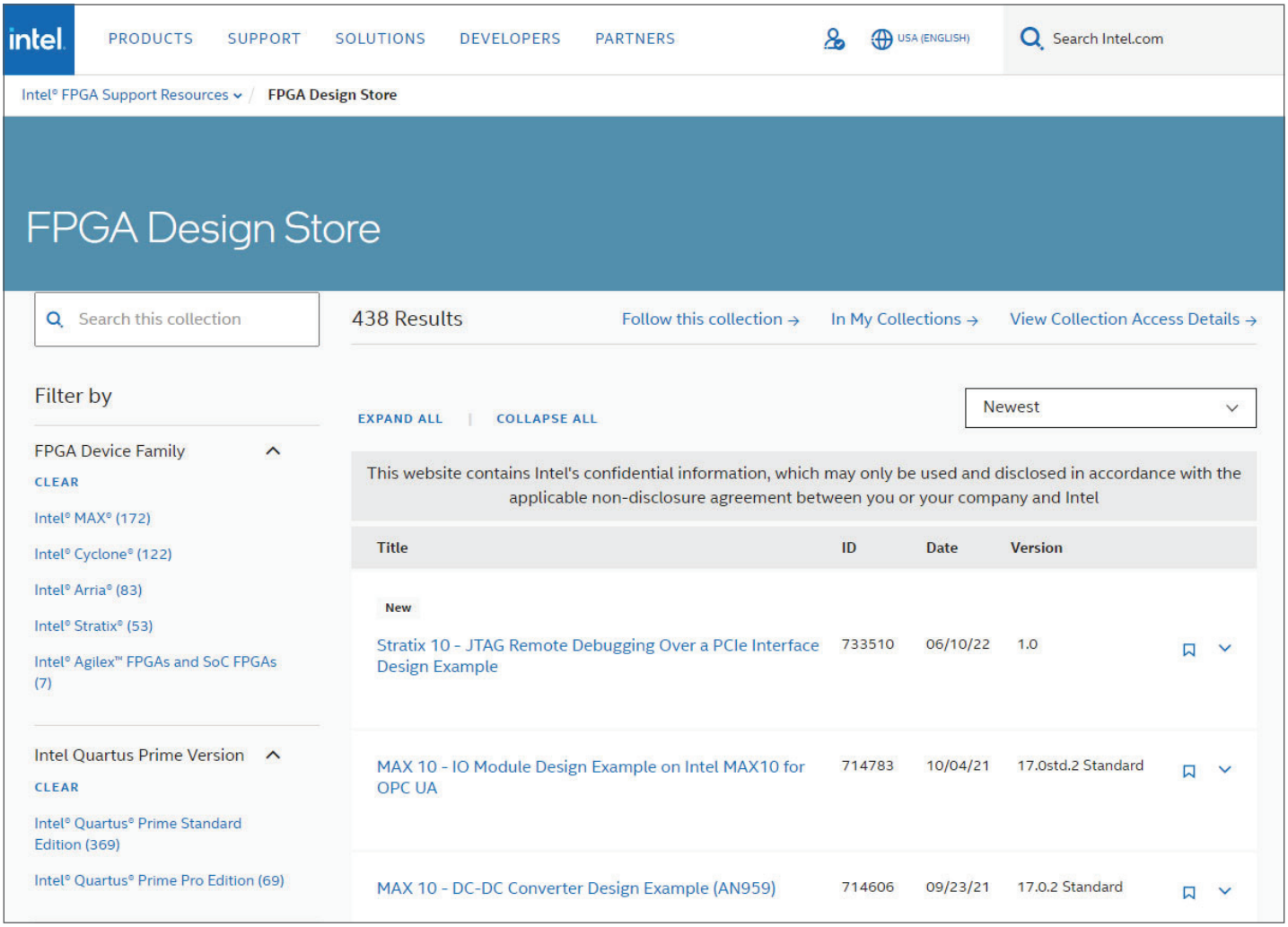
Design Store

fpgacloud.intel.com/devstore

The Design Store contains Intel and partner FPGA design examples to assist you in designing with Intel FPGAs and associated development tools. Design examples can be filtered by device family, development kit, Intel Quartus software versions, and IP for easy search. These design examples showcase a wide range of interface IP, core function IP, configuration, embedded, and end applications. New content is continuously added and updated for all product families.

Check out the Design Store now.

Design Example Search



Intel FPGA and Partner Development Kits

intel.com/devkits

Intel FPGA development kits provide a complete, high-quality design environment for engineers. These kits help simplify the design process and reduce time to market. Development kits include software, reference designs, cables, and programming hardware. Intel FPGA and partner development kits are listed below. For more details about these development kits or other older development kits that are available, check out our online development kits page at intel.com/devkits.

Product and Vendor Name	Description
Intel Agilex FPGA Kits	
Intel Agilex 7 FPGA F-Series Development Kit **Intel**	This kit allows you to design and develop your Intel Agilex 7 FPGA F-Series design, and includes all hardware and software needed to take advantage of the performance and capabilities of the Intel Agilex 7 FPGA F-Series with E-Tile and P-Tile. This PCIe form factor board can be used to develop and test PCI Express 4.0 designs, and external memory subsystems consisting of DDR4 and QDR IV memories. The kit also includes two QSFPDD connectors supporting both optical and electrical interfaces.
Intel Agilex 7 FPGA I-Series Development Kit **Intel**	The Intel Agilex 7 FPGA I-Series development kit delivers a complete prototyping and reference platform for designs needing PCIe 5.0 (32 GT/s), CXL v1.1, or 400G Ethernet connectivity. The Intel Agilex 7 FPGA I-Series Transceiver SoC development kit delivers a complete design environment that includes both hardware and software for developing with Intel Agilex 7 FPGA I-Series that contain 4x F-Tiles and 6 x F -Tiles.
Intel Stratix 10 FPGA Kits	
Intel Stratix 10 GX FPGA Development Kit **Intel**	This kit provides a complete design environment including all hardware and software needed to take advantage of the performance and capabilities of the Intel Stratix 10 GX FPGA. This kit can be used to develop and test PCI Express 3.0 designs, memory subsystem consisting of DDR4, DDR3, QDR IV, and RLDRAM III memories, and develop modular and scalable designs using FPGA mezzanine card (FMC) connectors.
Intel Stratix 10 GX Transceiver Signal Integrity Development Kit **Intel**	This kit provides a complete design environment including all hardware and software needed to take advantage of the performance and capabilities of the Intel Stratix 10 GX FPGA. This kit can be used to evaluate transceiver channel performance, generate and verify pseudo-random binary sequence (PRBS), and dynamically change the channel's differential output voltage (VoD), pre-emphasis, and equalization settings.
Intel Stratix 10 SX SoC Development Kit **Intel**	The kit offers a quick and simple approach for developing custom Arm processor-based SoC designs. It offers memory options, such as HiLo DDR4 and DDR4 SODIMM. There are also two FMC+ low-pin-count connectors and two quad small form factor pluggable (QSFP) connectors for transceiver channel performance. More notably, the kit offers two HPS peripheral daughtercards to expand the capabilities.
Intel Stratix 10 TX Signal Integrity Development Kit **Intel**	This kit offers a complete design environment for developing on the Intel Stratix 10 TX FPGA. It can evaluate E-Tile transceiver channel performance up to 58 Gbps PAM4 and 30 Gbps NRZ. The board has different QSFP-DD, FMC+, MXP, and SMA connectors for networking applications. It can also be used for jitter analysis and to verify physical medium attachment (PMA) compliance for 10/25/50G/100G/200G/400G Ethernet and other major standards.
Intel Stratix 10 MX FPGA Development Kit **Intel**	This kit can be used to test and develop designs using the Intel Stratix 10 MX FPGA. PCIe 3.0 designs can be developed as the board contains a PCIe end point connector and a PCIe root port connector. The board also contains a DIMM socket and HiLO connector for expanded memory capability.
S10VG4 **BittWare Inc.**	This PCI Express card is based on the Intel Stratix 10 FPGA and is ideal for high-density data center applications. BittWare's Viper platform offers support for large FPGA loads, up to 32 GB of DDR4 SDRAM, and 4x100 Gbps Ethernet. The card is enabled for high-speed networking with four front panel QSFP+ cages, each supporting 40/100GbE or four 10/25GbE channels. Serial expansion is available through two UltraPort SlimSAS connectors. A 1GbE interface, a pulse-per-second (PPS) input, and a USB interface are available for debug and support. The board's flexible memory configuration includes four DIMM sites that support DDR4 SDRAM and QDR.
Nallatech 520 **Nallatech**	This is a PCI Express accelerator card based on the Intel Stratix 10 FPGA designed to address a range of compute-intensive and latency-critical applications including machine learning, gene sequencing, oil and gas, and real-time network analytics. This introduces the ground-breaking single precision floating-point performance of up to 10 TFLOPS per device.

Product and Vendor Name	Description
Intel MAX 10 FPGA Kits	
Intel MAX 10 FPGA Nios II Embedded Evaluation Kit (NEEK) **Terasic**	This kit is a full featured embedded evaluation kit based on the Intel MAX 10 device family. The kit delivers an integrated platform that includes hardware, design tools, IP, and reference designs for developing a wide range of applications. This kit allows developers to rapidly customize their processor and IP to suit their specific needs, rather than constraining their software around the fixed feature set of the processor. The kit features a capacitive LCD multimedia color touch panel, which natively supports multi-touch gestures. An eight megapixel digital image sensor, ambient light sensor, and three-axis accelerometer make up this rich feature set, along with a variety of interfaces connecting the kit to the outside for Internet of Things (IoT) applications across markets.
Intel MAX 10 FPGA Development Kit **Intel**	This kit offers a comprehensive general-purpose development platform for many markets and applications, such as industrial and automotive. This fully featured development kit includes a 10M50DAF484C6G device, DDR3 memory, 2X 1 GbE, high-speed mezzanine card (HSMC) connector, quad serial peripheral interface, 16 bit digital-to-analog converter (DAC), flash memory, and 2X Digilent Pmod Compatible headers.
Intel MAX 10 FPGA Evaluation Kit **Intel**	The 10M08 evaluation board provides a cost-effective entry point to Intel MAX 10 FPGA design. The card comes complete with an Arduino header socket, which lets you connect a wide variety of daughtercards. Other features include an Intel MAX 10 10M08SAE144C8G device, Arduino shield expansion, access to 80 I/O through-holes, and a prototyping area.
DECA Intel MAX 10 FPGA Evaluation Kit **Arrow**	DECA is a full-featured evaluation kit featuring a 10M50DAF484C6G device. The kit includes a BeagleBone-compatible header for further I/O expansion, a variety of sensors (gesture/humidity/ temperature/CMOS), MIPI CSI-2 camera interface, LEDs, push buttons, and an onboard Intel FPGA Download Cable II.
Mpression Odyssey Intel MAX 10 FPGA IoT Evaluation Kit **Macnica**	The Macnica Intel MAX 10 FPGA evaluation kit connects and controls your FPGA design via Bluetooth using the Mpression Odyssey Smartphone application. This kit also includes a10M08U169C8G device, SDRAM, Arduino shield expansion capability, and Bluetooth SMART connectivity module.
Stratix V FPGA Kits	
Stratix V Advanced Systems Development Kit **Intel**	This kit is a complete systems design environment that includes both the hardware and software needed to begin architecture development and system design using Stratix V FPGAs. The PCI Express-based form factor utilizes a x16 edge connector, and includes high memory bandwidth to DDR3, QDR II+, and serial memory. Multiple high-speed protocols are accessible through FMC and HSMC connections. A one year license for the Intel Quartus Prime Software is available with this kit.
Stratix V GX FPGA Development Kit **Intel**	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix V GX FPGA. This kit includes the PCI Express x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, and SDI interfaces. Memory includes one x72 DDR3 SDRAM, one RLDRAM II x18 QDR II+ SRAM, and flash memory. This kit also includes two SMA connectors for a differential transceiver output. Several programmable oscillators are available and other user interfaces include three user push buttons, one 8-position DIP switch, 16 user LEDs, an LCD display, and power and temperature measurement circuitry.
Transceiver Signal Integrity Development Kit, Stratix V GX Edition **Intel**	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include seven full-duplex transceiver channels with SMA connectors, two 14G backplane connectors (from Amphenol and Molex), four programmable clock oscillators, four user push buttons, one 8-position DIP switch, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, an embedded Intel FPGA Download Cable, and JTAG interfaces.
Transceiver Signal Integrity Development Kit, Stratix V GT Edition **Intel**	The Stratix V GT Transceiver Signal Integrity Development Kit provides a platform for electrical compliance testing and interoperability analysis. The accessibility to multiple channels allows for real-world analysis as implemented in the system with transceiver channels available through SMA and popular backplane connectors. This development kit can be used for evaluation of transceiver link performance up to 25.7 Gbps, generation and checking pseudo-random binary sequence (PRBS) patterns via an easy-to-use GUI that does not require the Intel Quartus Prime Software, access advanced equalization to fine-tune link settings for optimal bit error ratio (BER), jitter analysis, and verifying physical media attachment (PMA) interoperability with Stratix V GT FPGAs for targeted protocols, such as CEI-25/28G, CEI-11G, PCI Express 3.0, 10GBASE-KR, 10 Gigabit Ethernet, XAUI, CEI-6G, Serial RapidIO, HD-SDI, and others. You can use the built-in high speed backplane connectors to evaluate custom backplane performance and evaluate link BER.
100G Development Kit, Stratix V GX Edition **Intel**	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through one x18 QDR II and six x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 12.5 Gbps, and verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCI Express (1.0, 2.0, and 3.0), and other major standards. This kit can also validate interoperability between optical modules, such as SFP, SFP+, QSFP, and CFP.
DSP Development Kit, Stratix V Edition **Intel**	The DSP Development Kit, Stratix V Edition provides a complete design environment that includes all the hardware and software you need to begin developing DSP intensive FPGA designs immediately. The development kit is RoHS-compliant. You can use this development kit to develop and test PCI Express designs at data rates up to 3.0, develop and test memory subsystems for DDR3 SDRAM or QDR II SRAM memories, and use the HSMC connectors to interface to one of over 35 different HSMCs provided by Intel partners, supporting protocols such as Serial RapidIO, 10 Gbps Ethernet, SONET, CPRI, OBSAI, and others.

Product and Vendor Name	Description
Intel Arria 10 FPGA Kits	
Intel Arria 10 FPGA Development Kit **Intel**	This kit provides a complete design environment including hardware and software for prototyping and testing high-speed serial interfaces to an Intel Arria 10 GX FPGA. This kit includes the PCI Express x8 form factor, two FMC connectors for expandability, Ethernet, USB, and SDIs. The board includes one HiLo connector for plugging in DRAM and SRAM daughtercards. Supported daughtercard formats include DDR4 x72 SDRAM, DDR3 x72 SDRAM, RLDRAM 3 x36, and QDR IV x36 SRAM. The board includes SMA connectors for transceiver output, clock output, and clock input. Several programmable oscillators are available and other user interfaces include user push buttons, dual in-line package (DIP) switches, bi-color user LEDs, an LCD display, power, and temperature measurement circuitry. This development kit comes with a one-year license for the Intel Quartus Prime Software.
Intel Arria 10 FPGA Signal Integrity Kit **Intel**	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include six full-duplex transceiver channels with 2.4 mm SMA connectors, four full-duplex transceiver channels to Amphenol Xcede+ backplane connector, four full-duplex transceiver channels to C form factor pluggable (CFP2) optical interface, four full-duplex transceiver channel to QSFP+ optical interface, one transceiver channel to SFP+ optical interface, and ten full-duplex transceiver channels to Samtec BullsEye high-density connector. This board also includes several programmable clock oscillators, user push buttons, DIP switches, user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, Ethernet, an embedded Intel FPGA Download Cable II, and JTAG interfaces. This development kit comes with a one-year license for the Intel Quartus Prime Software.
Intel Arria 10 SoC Development Kit **Intel**	This kit offers a quick and simple approach for developing custom Arm processor-based SoC designs. The Intel Arria 10 SoCs offers full software compatibility with previous generation SoCs, a broad ecosystem of Arm software and tools, and an enhanced FPGA and DSP hardware design flow. This kit includes an Intel Arria 10 10AS066N3F40I2SG SoC, PCI Express 3.0 protocol support, a dual FMC expansion headers, two 10/100/1000 SGMII Ethernet ports, one 10/100/1000 RGMII Ethernet port, two 10GbE small form factor pluggable (SFP) cages, two 1GB DDR4 HPS HiLo memory card, DDR4 SDRAM, NAND, quad SPI, SD/MICRO boot flash cards, character LCD, display port, and SDI port.
Attila Instant-Development Kit Intel Arria 10 FPGA FMC IDK **REFLEX**	This kit provides out-of-the-box experience, combining compact hardware platform and an efficient intuitive software environment. This kit is designed for high-performance serial transceiver applications using Intel Arria 10 GX 1150 KLEs. Hardware, software design tools, IP, and pre-verified reference designs included. Its unique installation and GUI allows an immediate start, and its reference designs enable fast turn-around designs, shortening and securing the developments.
Alaric Instant-Development Kit Intel Arria 10 SoC FMC IDK **REFLEX**	This kit provides out-of-the-box experience, combining compact hardware platform and an efficient intuitive software environment. This kit is designed for high-performance serial transceiver applications using an Intel Arria 10 SoC with 660 KLEs and an Arm dual-core Cortex-A9 MPCore. Its unique installation and GUI allows an immediate start, and its reference designs enable fast turn-around designs, shortening and securing the developments.
Nallatech 510T **Nallatech**	Nallatech 510T is an FPGA co-processor that is designed to deliver ultimate performance per watt for compute-intensive data center applications. The 510T is a GPU-sized 16-lane PCI Express 3.0 card featuring two of Intel's new floating-point enabled Intel Arria 10 FPGAs delivering up to 16 times the performance of the previous generation[†]. Applications can achieve a total sustained performance of up to 3 TFLOPS.
Intel Cyclone 10 FPGA Kits	
Intel Cyclone 10 LP Evaluation Kit **Intel**	This kit provides an easy-to-use platform for evaluating Intel Cyclone 10 LP FPGA technology and Intel Enpirion regulators. This evaluation board enables you to develop designs for Intel Cyclone 10 LP FPGAs via Arduino UNO R3 shields, Digilent Pmod Compatible cards, GPIOs, or Ethernet connector. This kit also measures key Intel Cyclone 10 LP FPGA power supplies and reuse the kit's PCB schematic as a model for your design.
Intel Cyclone 10 GX FPGA Development Kit **Intel**	This kit is an ideal starting point for developing applications, such as embedded vision, factory automation, and surveillance. With this development kit, you can develop Intel Cyclone 10 GX FPGA-based designs with expansion through PCIe 2.0, USB 3.1, SFP+, and RJ-45.

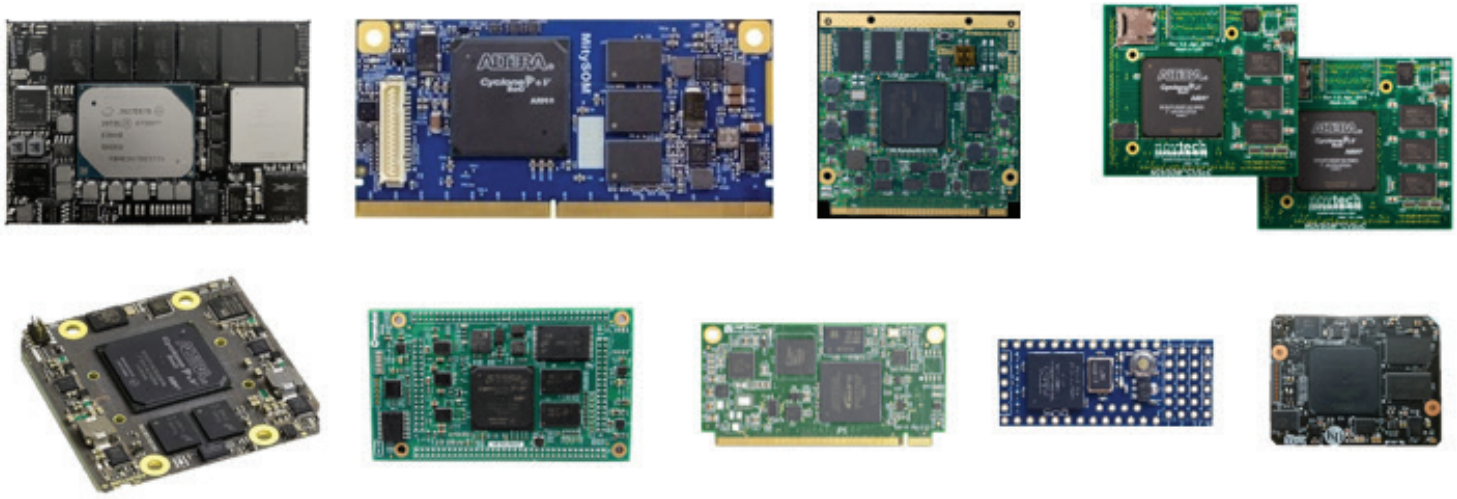
Product and Vendor Name	Description
Arria V FPGA and SoC Kits	
Arria V GX Starter Kit, Arria V GX Edition **Intel**	This kit provides a low-cost platform for developing transceiver I/O-based Arria V GX FPGA designs. This kit includes the PCI Express x8 form factor, one HSMC connector, a 32 bit DDR3 SDRAM device, one-channel high-speed transceiver input and output connected to SMAs, HDMI output, SDI input and output, 16x2 LCD display, and flash memory.
Arria V SoC Development Kit and SoC Embedded Design Suite **Intel**	The Arria V SoC Development Kit offers a quick and simple approach to develop custom Arm processor-based SoC designs. Intel's midrange, transceiver-based Arria V FPGA fabric provides the highest bandwidth with the lowest total power for midrange applications such as remote radio units, 10G/40G line cards, medical imaging, broadcast studio equipment, and the acceleration of image- and video-processing applications. This development kit includes the SoC Embedded Design Suite software development tools. The development board has PCI Express 2.0 x4 lanes (endpoint or rootport), two FMC expansion headers, dual Ethernet PHYs, and various DRAM and flash memories.
Cyclone V FPGA and SoC Kits	
Cyclone V E FPGA Development Kits **Intel**	The Cyclone V E Development Kit offers a comprehensive general-purpose development platform for many markets and applications, including industrial, networking, military, and medical applications. The kit features an Intel Cyclone V device and a multitude of onboard resources including multiple banks of DDR3 and LPDDR2 memory, LCD character display, LEDs, user switches, USB, and RJ-45 connectors. The Cyclone V E FPGA Development Kit gives industrial equipment designers greater flexibility in implementing real-time Ethernet communications with industrial Ethernet IP cores.
Cyclone V GT FPGA Development Kit **Intel**	This kit can be used to prototype Cyclone V GT FPGA or Cyclone V GX FPGA applications. It offers a quick and simple way to develop low-cost and low-power system-level designs and achieve rapid results. This kit supports a myriad of functionalities, such as FPGA prototyping, FPGA power measurement, transceiver I/O performance up to 5 Gbps, PCI Express 2.0 x4 (at 5 Gbps per lane), endpoint or rootport support.
Cyclone V SoC Development Kit **Intel**	The Cyclone V SoC Development Kit offers a quick and simple approach to develop custom Arm processor-based SoC designs accompanied by Intel's low-power, low-cost Cyclone V FPGA fabric. This kit supports a wide range of functions, such as processor and FPGA prototyping and power measurement, industrial networking protocols, motor control applications, acceleration of image- and video-processing applications, PCI Express x4 lane with ~1,000 MBps transfer rate (endpoint or rootport).
Cyclone V GX Starter Kit **Terasic Technologies**	The Cyclone V GX Starter Kit offers a robust hardware design platform based on Cyclone V GX FPGA. This kit is optimized for the lowest cost and power requirement for transceiver applications with industry-leading programmable logic for ultimate design flexibility. The Cyclone V Starter Kit development board includes hardware, such as Arduino Header, onboard Intel FPGA Download Cable circuit, audio and video capabilities, and an onboard HSMC connector with high-speed transceivers that allows for an even greater array of hardware setups.
DE0-Nano-SoC Kit **Terasic Technologies**	The DE0-Nano-SoC Kit combines a robust, Cyclone V SoC-based development board and interactive reference designs into a powerful development platform. This low-cost kit is an interactive, web-based guided tour that lets you quickly learn the basics of SoC development and provides an excellent platform on which to develop your own design. The board includes a Gigabit Ethernet port, USB 2.0 OTG port, SD card flash, 1 GB DDR3 SDRAM, an Arduino header, two 40-pin expansion headers, onboard Intel FPGA Download Cable circuit, 8-channel A/D converter, accelerometer, and much more.
MAX V CPLD Kits	
MAX V CPLD Development Kit **Intel**	This low-cost platform will help you quickly begin developing low-cost, low-power CPLD designs. Use this kit as a stand-alone board or combined with a wide variety of daughtercards that are available from third parties. With this platform, you can develop designs for the 5M570Z CPLD and build upon example designs provided.
Stratix IV FPGA Kits	
100G Development Kit, Stratix IV GT Edition **Intel**	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through four x18 QDR II and four x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 11.3 Gbps, verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCI Express (1.0, 2.0, and 3.0), and other major standards. This kit can also validate interoperability between optical modules, such as SFP, SFP+, QSFP, and CFP.

Product and Vendor Name	Description
Cyclone IV FPGA Kits	
Cyclone IV GX FPGA Development Kit **Intel**	This kit provides a comprehensive design environment that allows you to quickly develop low-cost and low-power FPGA system-level designs. This kit includes the PCI Express short card form factor, two HSMC connectors, and a 10/100/1000 Mbps Ethernet interface. Onboard memory includes 128 MB DDR2 SDRAM, 64 MB flash, and 4 MB SSRAM. This kit also includes SMA connectors, and 50 MHz, 100 MHz, and 125 MHz clock oscillators, as well as user interfaces including push buttons, LEDs, and a 7-segment LCD display.
DEO-Nano Development Board **Terasic Technologies**	The DE0-Nano Development Board is a compact-sized FPGA development platform suited for prototyping circuit designs such as robots and "portable" projects. The board is designed to be used in the simplest possible implementation targeting the Cyclone IV device up to 22,320 LEs. This kit allows you to extend designs beyond the DE0-Nano board with two external general-purpose I/O (GPIO) headers and allows you to handle larger data storage and frame buffering with onboard memory devices including SDRAM and EEPROM. This kit is lightweight, reconfigurable, and suitable for mobile designs without excessive hardware. This kit provides enhanced user peripheral with LEDs and push buttons and three power scheme options including a USB Mini-AB port, 2-pin external power header, and two DC 5-V pins.
Industrial Networking Kit **Terasic Technologies**	The Industrial Networking Kit (INK) offers a comprehensive development platform for industrial automation and applications. The kit consists of the DE2-115 board featuring the Cyclone IV device and dual 10/100/1000-Mbps Ethernet, 128 MB SDRAM, 8 MB flash memory, 2 MB SRAM, HSMC and GPIO connectors, USB 2.0, an SD card slot, switches and buttons, LEDs, 16x2 display, audio and video, and VGA-out. The kit also includes an Industrial Communications Board (ICB-HSMC) that supports RS-485, RS-232, CAN, and additional I/O expansion.
DE2-115 Development and Education Board **Terasic Technologies**	This board is part of the DE2 educational development board series and features the Cyclone IV E EP4CE115 FPGA. The DE2-115 offers an optimal balance of low cost, low power, and a rich supply of logic, memory and DSP capabilities, as well as interfaces to support mainstream protocols including GbE. A HSMC connector is provided to support additional functionality and connectivity via HSMC daughtercards and cables.
MAX II CPLD Kits	
MAX II/MAX IIZ Development Kit **System Level Solutions**	This board provides a hardware platform for designing and developing simple and low-end systems based on MAX II or MAX IIZ devices. The board features a MAX II or MAX IIZ EPM240T100Cx or EPM240ZM100Cx device with 240 LEs and 8,192 bits of user flash memory (UFM). The board also supports vertical migration into EPM570T100Cx devices with 570 LEs and 8,192 bits of UFM.

FPGA-Based SoM Partner Ecosystem

intel.com/som

System on modules (SoMs) provide a compact, pre-configured solution with FPGA, memory, and software which is perfect for prototyping, proof-of-concept, and initial system development and production. SoMs enable you to focus on development of your IP, algorithms, and human/mechanical interfaces rather than spending time on the fundamentals of the processor and electrical system and software bring-up. In many cases, SoMs can also make sense for full system production.



Customer Benefits

- Faster time to market by off-loading complex board design
- Production-ready hardware for immediate deployment
- Versatile product design and application fit from various partners
- Minimize component supplier management

Target Application

- General embedded applications
- Industrial PC, factory automation, and control applications
- Machine vision, surveillance camera, and retail applications
- Networking and security applications
- Test and measurement equipment

Related Links

- Browse FPGA-based SoMs on Intel Partner Showcase
- Read the Agilex 5 SoM Solution Brief

Intel Partner Alliance Program

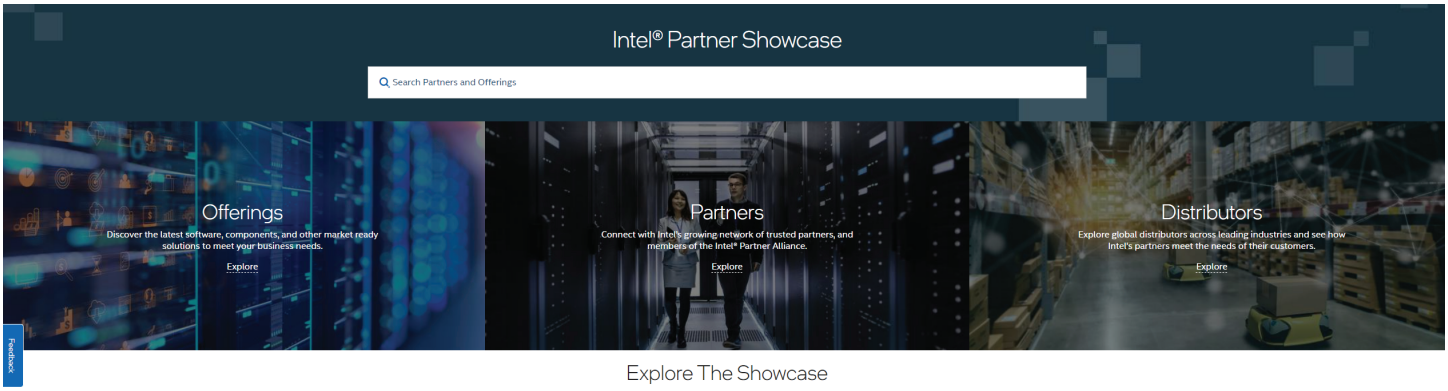
intel.com/partneralliance

The Intel Partner Alliance is a program designed to enhance the value, relevance, and the experience we deliver to our partners. The unification of former Intel partner programs such as the Design Solutions Network and the FPGA Partner Program, to name a few, will allow Intel and its partners to continue driving the industry to innovate solutions with powerful technology. These investments will help enable disruption and accelerate new market opportunities in an increasingly data-centric world. From leading-edge technologies to sophisticated sales enablement and powerful partner networking, the Intel Partner Alliance will connect partners to a world of innovation.

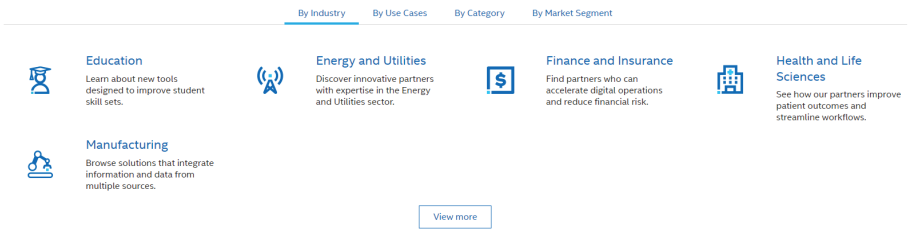
Join the Intel Partner Alliance

Visit the Intel® Partner Showcase to connect with thousands of partners, opening the door to matchmaking opportunities to grow your business and innovate. Browse a selection of FPGA IP, boards, design services, and other offerings from our partners – the fastest way to find products, solutions, and Intel Partner Alliance partners that meet your business needs.

Visit the Intel ® Partner Showcase



Explore The Showcase



Training Overview

Intel FPGA Technical Training

Intel FPGA technical training offers many ways to learn. Sharpen your FPGA design skills today! All public training is free to attend.

On-Demand Training	Learn FPGA Design Topics from Expert Instructors	Webinars, Workshops and Quick Videos
Learn at your convenience with our on-demand eLearning, all for FREE! The duration of each eLearning session typically ranges from approximately 30 minutes to one hour. A convenient player makes it easy to skip to the sections that interest you most. Please click to view our learning plans, designed to guide you through a set of e-learning modules, each offering a well-structured learning path. (Note: It requires logging in to the learning.intel.com website first)	Learn FPGA design topics from expert instructors and earn badges for your achievements, all for FREE! Classes are taught as either one or a series of two half-day sessions. The virtual classroom allows you to attend from work or home. During class, access to a remote lab environment is provided – which means no setup is required to attend.	Webinars and workshops are shorter events that offer an overview of the subject being taught. Join us and learn something new in these informative sessions. These short how-to YouTube videos teach specific skills to help solve your issues. Check out the Intel FPGA Quick Videos page or the Engineer to Engineer: How-To YouTube Channel.

Instructor-Led Trainings

Instructor-Led and Virtual Classes (Note: It requires logging in to the learning.intel.com website first)

Course	Description
Beginner Workshop for Intel FPGAs	This course introduces the FPGA device in an easy-to understand manner for people who are completely new to the world of FPGAs such as FPGA. It uses the Intel Quartus Prime software tool to provide a practical approach towards utilizing' FPGAs for design in the world of hardware. It introduces FPGAs, their architecture, the basic tools in Intel Quartus Prime software that is used for FPGA design.
Verilog HDL Basics	This class is a general introduction to the Verilog language and its use in programmable logic design, covering the basic constructs used in both the simulation and synthesis environments. By the end of this course, you will have a basic understanding of the Verilog module, data types, operators and assignment statements needed to begin creating your own designs, using both behavioral and structural approaches. In the hands-on laboratory sessions, you will get to practice the knowledge you have gained by writing simple but practical designs. You will check your designs by compiling in the Intel Quartus Prime software and simulating in the Questa-Intel FPGA Edition software.
Verilog HDL Advanced	You will learn efficient coding techniques for writing synthesizable Verilog for Intel FPGAs and CPLDs. You will gain experience in behavioral and structural coding while learning how to effectively write common logic functions including registers, memory, and arithmetic functions. You will learn how to parameterize your Verilog design, increasing flexibility and reusability. You will be introduced to testbenches and the constructs used when building them.
Using Intel Quartus Software	You will learn how to use the Intel Quartus Prime Pro Edition software & correlate these steps to the general flow of an FPGA design process. You'll create a new project, input new or existing design files, and compile your project. Learn how to search for compilation information, use settings and assignments to adjust the results of compilation, and go through an overview to migrate another vendor's design to an Intel Quartus Prime Pro design.
Intel® Simics® Simulator for Intel FPGAs	Intel Simics Simulator for Intel FPGAs is used to test your software early on in the development process. This training covers the functionalities for the simulator that include hardware and software inspection, dynamic system configuration, hardware modeling tools, scripting, and a rich set of other features.

Course	Description
Intel Stratix 10 and Intel Agilex 7 SoC FPGA Basics	This class will teach you how to design with Intel Stratix 10 and Intel Agilex 7 SoC FPGAs using the Intel Quartus Prime software and how to develop software for these devices. You will get an an overview of the Arm Cortex-A53 and the peripherals present in the hard processor system. You will learn to add and configure the processor component in a Platform Designer system. You will then learn to implement and configure the first-stage and second-stage bootloaders (based on U-Boot), including how to append the first-stage bootloader and how to build the Linux OS. You will learn the boot stages of each SoC FPGA family and how to gather all the pieces for the implementation.
Introduction to the Nios V Processor	Nios V processor is the next generation soft core processor based on the open-source RISC-V instruction set, designed for Intel FPGA devices. One or more soft processors can be instantiated in a device's programmable fabric allowing designers to add a microcontroller or microprocessor core to a solution, Nios V processor IP can be added through the device's programmable fabric using Intel Quartus Software and Ashling* RISCFree IDE for Intel FPGAs.
Intel Quartus Prime Software Debug Tools: Signal Tap	This course introduces and focuses on the Signal Tap embedded logic analyzer, one of the many debug tools included in the Intel Quartus Prime software. You'll learn how including the logic analyzer in your FPGA design makes it easy to debug your design quickly by triggering on internal hardware events and monitoring tapped signals, decreasing your overall design development time. You'll gain experience with using Signal Tap through hands-on lab exercises utilizing the tool in a real design.
Introduction to Platform Designer: Building Systems	This class will teach you the basics of how to build embedded system designs quickly for Intel FPGA devices using the Platform Designer system-level integration tool, part of the Intel Quartus Prime software. Platform Designer can be used as a design entry method for any FPGA design, though its use is required if you are implementing a Nios processor or the Hard Process System (HPS) in an SoC device. You will become proficient with using Platform Designer and learn how to quickly integrate "off-the-shelf" IP into a system.
Intel FPGA Timing Analysis: Lecture	You will learn how to constrain and analyze a design for timing using the Timing Analyzer in the Intel Quartus Prime Pro software v.22.1. This includes writing Synopsys Design Constraint (SDC) files, generating various timing reports in the Timing Analyzer, and applying this knowledge to an FPGA design. Besides learning the basic requirements to ensure that your design meets timing, you will see how the Timing Analyzer makes it easy to create timing constraints to help you meet those requirements.
Intel FPGA Timing Analysis: Hands-On Labs	This workshop is a follow on to the Intel FPGA Timing Analysis: Lecture class. There will be a brief review of the SDC constraints learned in the previous class before starting the labs.
Intel FPGA Timing Closure: Lecture	This class teaches the techniques used by design specialists to close timing on designs that "push the envelope" of performance. Example techniques include thoroughly analyzing the design for common timing failures, adjusting settings and assignments according to tool recommendations, selecting the correct clock resources, and adjusting HDL code for optimal performance.
Intel FPGA Timing Closure: Hands-On Lab	This workshop is a follow on to the Intel FPGA Timing Closure: Lecture class. Your time during this workshop will mostly be spent using the Intel Quartus Prime Software to practice timing closure techniques. There will be a brief review of the timing closure techniques and reports learned in the previous class before starting the labs.

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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